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II YR EEE

UNIT - 4

SPECIAL IC's

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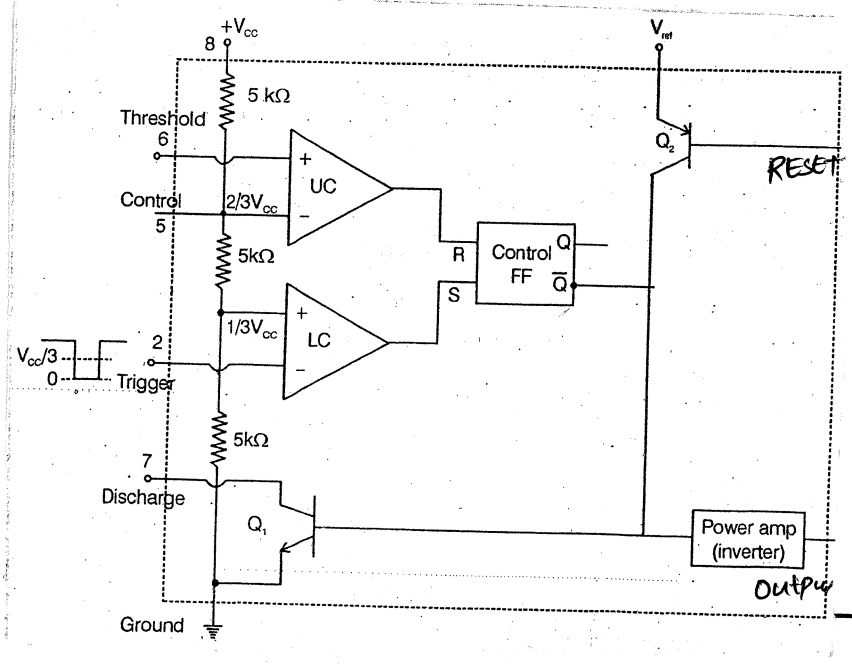
AP/ECE

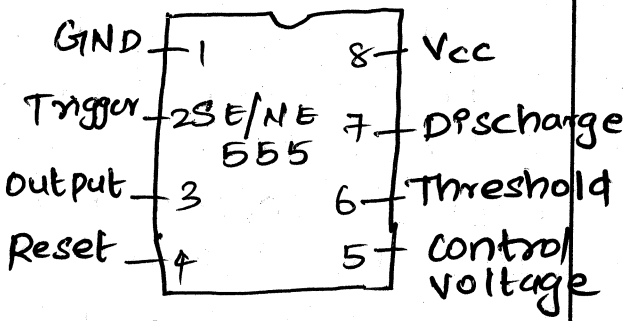
TIMER IC 555 and its modes of multivibrator and explain on it?

* 555 timer is a highly stable device for generating accurate time delay (or) oscillation.
* A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.
* It is designed to perform signal generation and specific timing
* Voltage range: +5V to +18V
* drive load : 200mA
* It is compatible with both TTL and CMOS logic circuits and op-amp based circuits

APPLICATIONS:

1. oscillator
2. pulse generator
3. Ramp and saluare wave generator
4. Monoshot multivibrator
5. Burglar alarm
6. Traffic light control
7. Voltage monitor





PIN DIAGRAM OF IC555

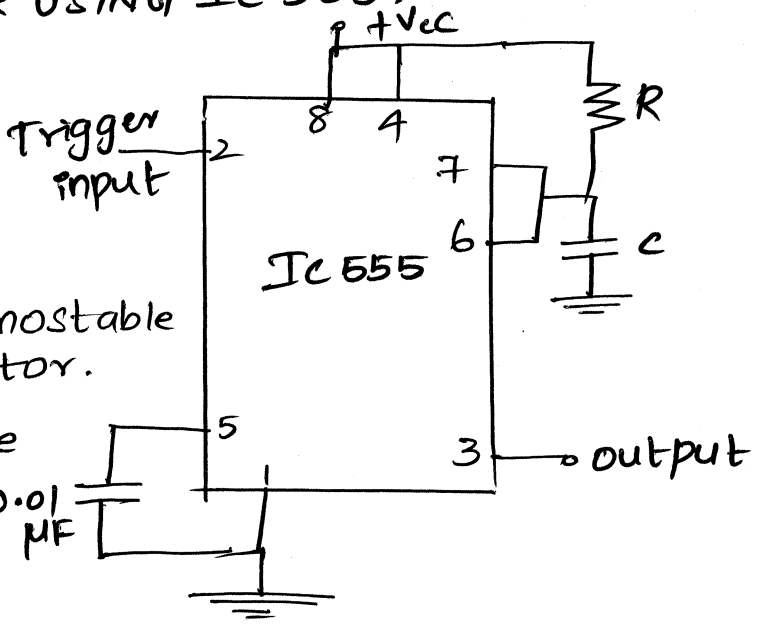
* The positive d.c power supply terminal is connected to pins (Vcc) and negative terminal is connected to pin 1 (GND)
* A control voltage input terminal accepts a modula-tion control input voltage applied externally.
* The (+) input terminal of the upper comparator is called **threshold terminal**
* The (-) input terminal of the Lower comparator is called **trigger terminal.**

OPERATION:

* In Standby mode, the output $\overline{Q}$ of the control FF is HIGH. This makes the output low because of power amplifier which is basically an inverter.
* When a negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator.
* At the negative going edge of the trigger, as the trigger passes through the output of the lower comparator goes HIGH and sets the control FF.

MONOSTABLE MULTIVIBRATOR USING IC 555:

* The Monostable multi Vibrator has one stable state and one-quest stable state.
* It is also known as monostable (or) one-shot multivibrator.
* It remains in its stable state until an impulse pulse triggers it into its quasi-stable state.



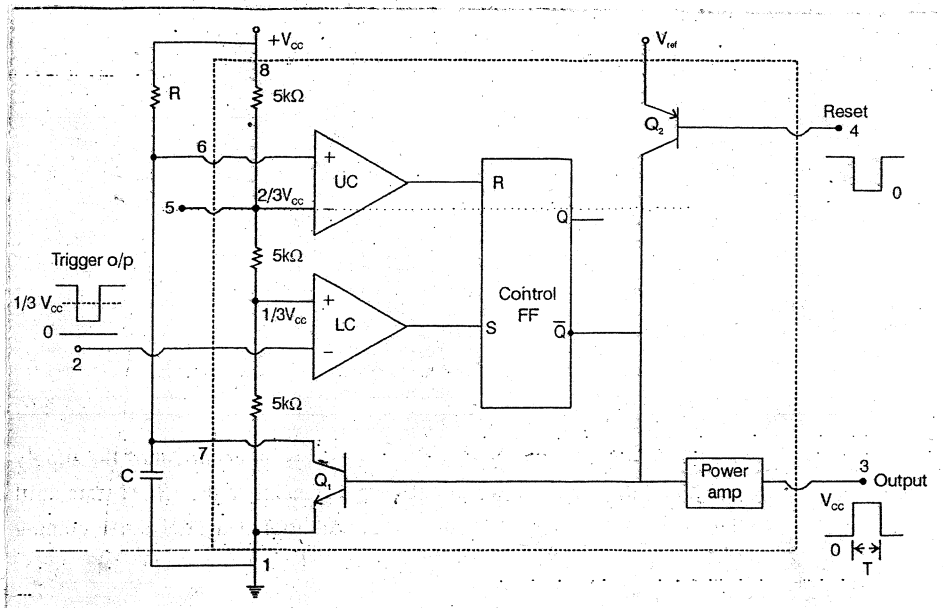


Fig.4.4 Timer in mono-stable operation with functional diagram

* In the standby mode, control FF holds transistor Q_1 ON, thus clamping the external timing capacitor C to ground.

ANALYSIS:

Voltage across the capacitor as given below:

$$V_c = V_{cc}\left(1 - e^{-t/RC}\right)$$

At $t = T$, $V_c = \frac{2}{3} V_{cc}$

$$\frac{2}{3} V_{cc} = V_{cc}\left(1 - e^{-T/RC}\right)$$

$$\frac{2}{3} = 1 - e^{-T/RC}$$

$$\frac{2}{3} - 1 = -e^{-T/RC}$$

$$\frac{-1}{3} = -e^{-T/RC}$$

Taking natural log on both sides

$$\ln\left(\frac{1}{3}\right) = \frac{-T}{RC}$$

$$-T = RC \ln\left(\frac{1}{3}\right)$$

$$\boxed{T = 1.1\,RC}$$

APPLICATIONS MULTIVIBRATOR USING 555:

(a) Pulse missing Detector
(b) Freqluency divider
(c) PWM application

(a) PULSE MISSING DETECTOR:

* input trigger is low
↓
emitter diode of the transistor Q is Forward Biased.
* The capacitor C gets clamped to few tenths of a volt.
* The timer output goes HIGH.

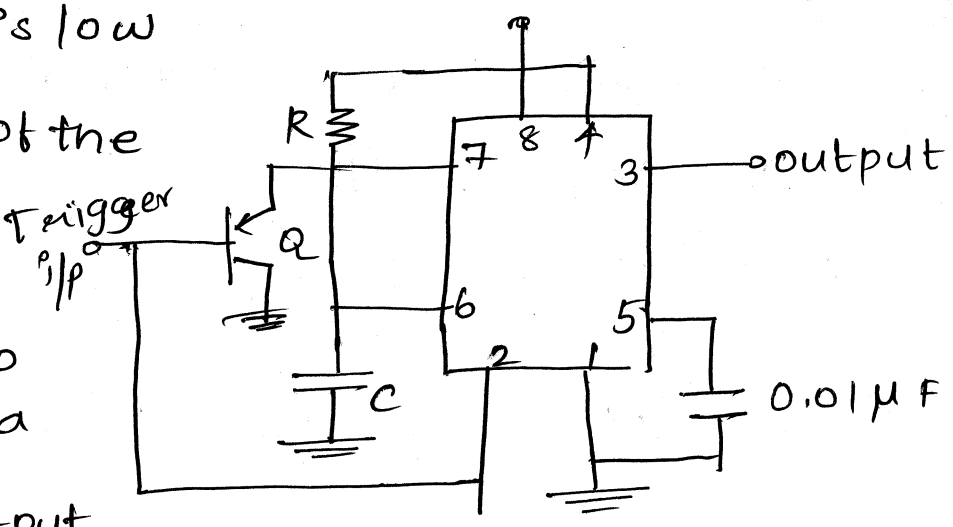


FIG: A MISSING PULSE DETECTOR MONOSTABLE CIRCUIT

* If the pulse misses the trigger input is High and transistor Q_1 is cutoff
* The 555 enters into normal state of monostable operation.
* The output goes LOW after time t of the monoshot
* This circuit can be used to detect missing heart beat. It can also be used for speed control and measurements.

(b) FREQUENCY DIVIDER:

* The monostable multivibrator when continuously triggered by a square wave signal can be used as a frequency divider.
* If the timing interval T of the monostable multivibrator is designed to be longer than the period of the triggering square-wave signal.
* The one-shot is triggered by the first negative edge of the square-wave input.
* During the second negative edge of the square wave, the output of monostable multi vibrator remains HIGH.
* During the third negative edge of the square wave, the monoshot once again triggers ON.

(c) PWM APPLICATION:

* The monostable multivibrator, when applied with a modulating control input signal at pin 5 can act as a pulse width modulator.
* The series of trigger pulses at pin 2 generates a series of output pulses.
* The duration of the output pulses are deter-mined by the triggering of the upper compa-rator, which in turn depends on the modula-ting signal input at pin 5.
* This is due to the fact that, the modulating signal is superimposed upon the voltage $\frac{2}{3}$ Vcc obtained through voltage divider circuit.

*The threshold level of the upper comparator thus changes, and the output pulse modulation occurs.

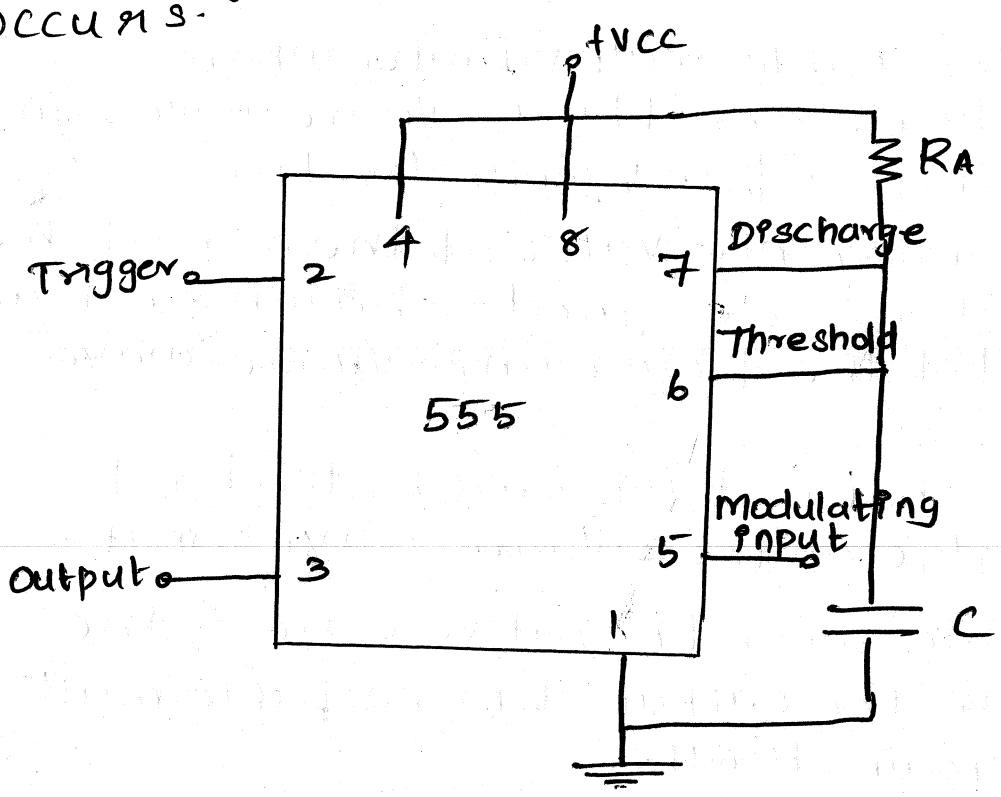


FIG: PULSE WIDTH MODULATOR USING MONOSTABL MULTIVIBRATOR

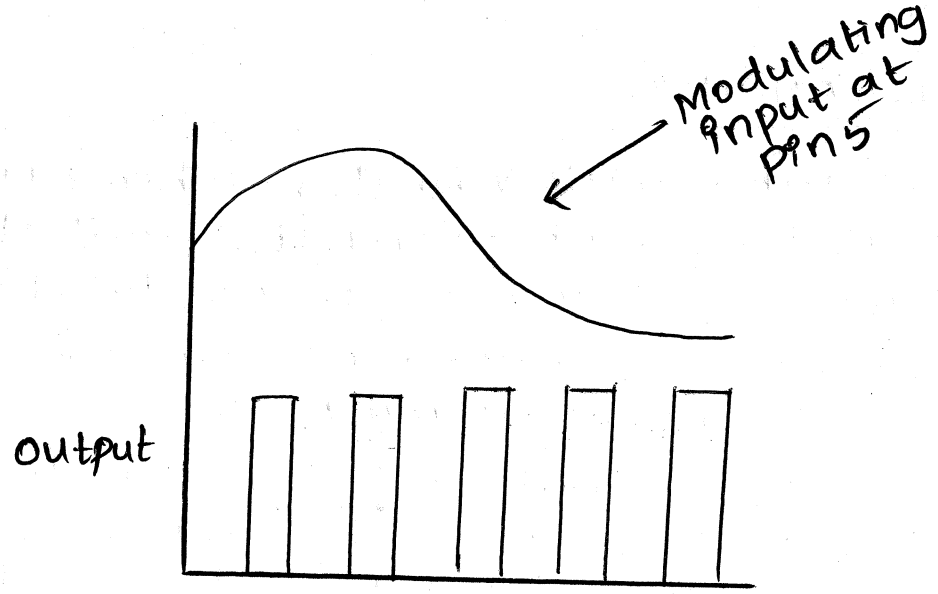


FIG: INPUT AND OUTPUT WAVEFORMS

*It may be noted from the output waveform that the pulse duration, that is, the duty cycle varies, keeping the frequency same as that of continuous input pulse train trigger.

ASTABLE MULTIVIBRATOR USING IC 555:

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* comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B.
* The discharge (pin 7) terminal is connected to the junction of R_A and R_B.
* Threshold (pin 6) and trigger (pin 2) terminals are connected to the VC terminal and control (pin 5) terminal is by passed to ground through 0.01 μF capacitor.

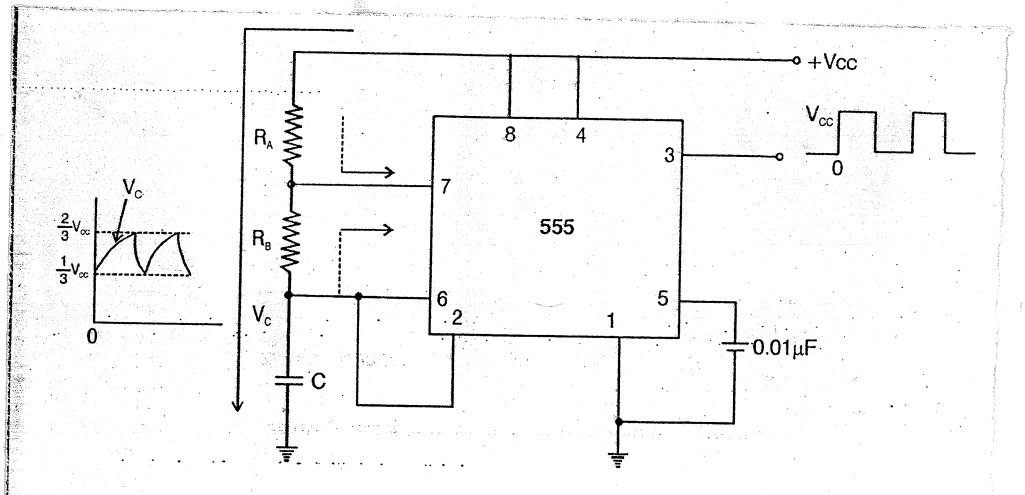


Fig.4.12 Astable multivibrator

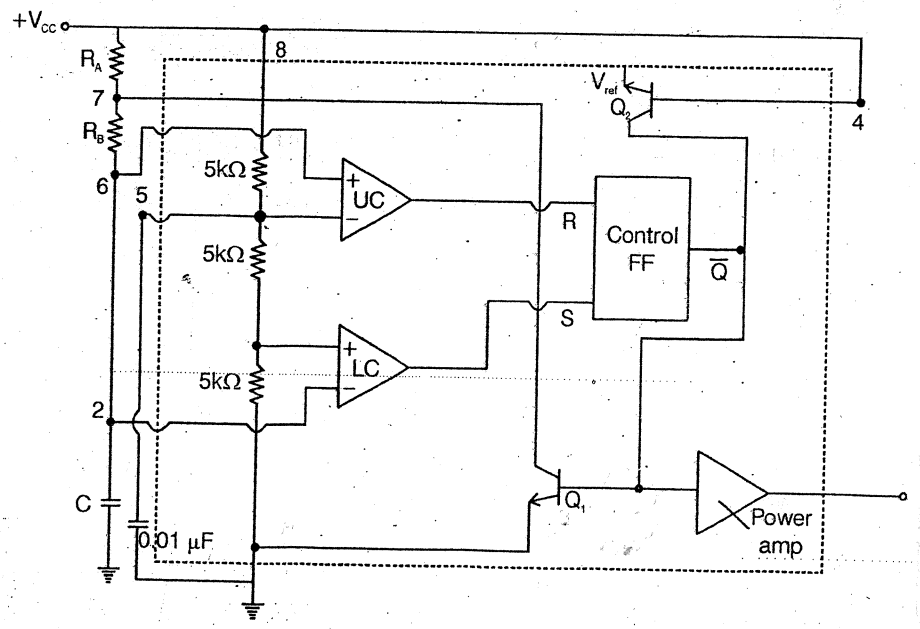


Fig.4.13 Functional diagram of astable multivibrator using 555 timer

* When the capacitor voltage reaches and rises above $\frac{2}{3}V_{cc}$ the upper comparators triggers and reset the control flipflop so that $\bar{Q}=1$.

* Q_1 transistor → ON

* Capacitor starts discharging towards ground through R_B and transistor Q_1 with the time constant time $R_B C$.

* During the discharge of timing capacitor c as it reaches $\frac{V_{cc}}{3}$, the lower comparators is triggered and this stage $S=1, R=0$ which turns $\bar{Q}=0$.

* The capacitor is charged and discharged between $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively.

ANALYSIS:

$$V_c = V_{cc}(1-e^{-t/RC})$$

$t=t_1$, $V_c=\frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}(1-e^{-t_1/RC})$$

$$\frac{2}{3} = 1-e^{-t_1/RC}$$

$$\frac{2}{3}-1 = -e^{-t_1/RC}$$

$$-\frac{1}{3} = -e^{-t_1/RC}$$

Taking natural log on both sides

$$\ln\left(\frac{1}{3}\right) = \frac{-t_1}{RC}$$

$$-t_1 = RC\ln\left(\frac{1}{3}\right)$$

$$\boxed{t_1 = 1.1RC}$$

At $t = t_2$, $V_C = \frac{1}{3} V_{CC}$

$$\frac{1}{3} V_{CC} = V_{CC}\left(1 - e^{-t_2/RC}\right)$$

$$\frac{1}{3} - 1 = -e^{-t_2/RC}$$

$$\frac{-2}{3} = -e^{-t_2/RC}$$

Taking natural log on both sides

$$\ln\left(\frac{2}{3}\right) = \frac{-t_2}{RC}$$

$$-t_2 = RC \ln\left(\frac{2}{3}\right)$$

$$\boxed{t_2 = 0.405\ RC}$$

$$t_{High} = t_1 - t_2$$

$$= 1.1RC - 0.405RC$$

$$= RC(1.1 - 0.405)$$

$$\boxed{t_{HIGH} = 0.69\ RC}$$

So for the given circuit

$$t_{High} = 0.69\ (R_A + R_B)\ C$$

$$t_{low} = 0.69\ R_B\ C$$

$$T = t_{HIGH} + t_{LOW}$$

$$= 0.69\ (R_A + R_B)\ C + 0.69\ R_B\ C$$

$$= 0.69\ R_A C + 0.69\ R_B C + 0.69\ R_B C$$

$$T = 0.69\ (R_A + 2R_B)\ C$$

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

The duty cycle D of the circuit is defined as the ratio of ON time to the total time period.

$$T = (t_{ON} + t_{OFF})$$

*In this circuit, when the transistor Q_1 is on the output goes low.

$$D\% = \frac{t_{low}}{T} \times 100$$

$$D\% = \frac{R_B}{R_A + 2R_B} \times 100$$

APPLICATIONS IN ASTABLE MODE:

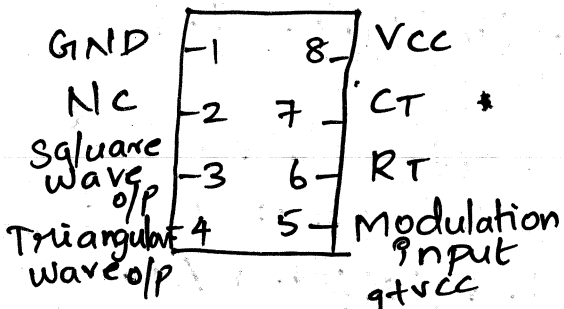
* FSK Generator
* Timer as a schmitt trigger.

UNIT-3

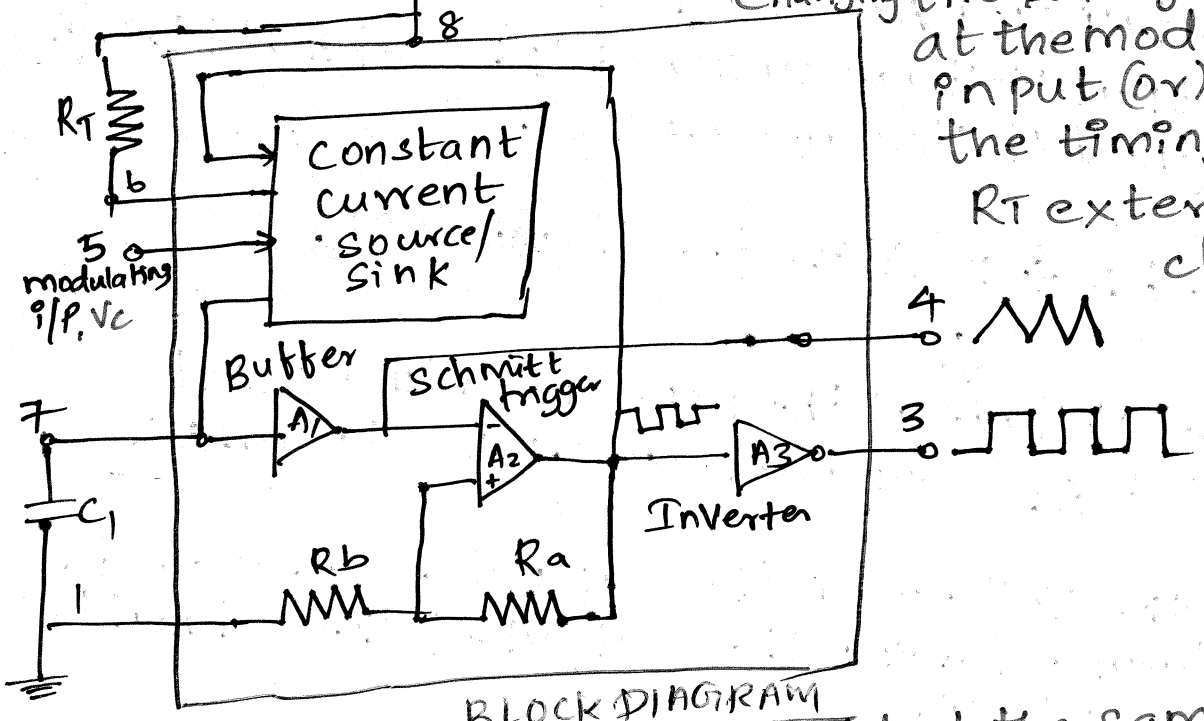
VOLTAGE CONTROLLED OSCILLATOR (VCO)

* A common type of Vco available in Ic form is Signetics NE/SE 566.
* The pin configuration and basic block diagram of 566 Vco are shown in this.

PIN DIAGRAM



* A timing capacitor C_T is linearly charged or discharged by a constant current source/sink.
* The amount of current can be controlled by changing the voltage Vc applied at the modulating input (or) by changing the timing Resistor R_T external to Ic chip.



BLOCK DIAGRAM

* The Voltage at pin 6 is held at the same Voltage as pin 5.
* Thus, if the modulating Voltage at pin 5 is increased, the Voltage at pin 6 also increases, resulting in less Voltage across R_T and thereby decreasing the charging current.

* A small capacitor of 0.001 μF should be connected between pin 5 and 6 to eliminate possible oscillations.

* A Vco is commonly used in converting low frequency signals such as EEGs, EKG into an audio frequency range.

* These audio signals can be transmitted over telephone lines or a two way radio communi-cation systems for diagnostic purposes or can be recorded on a magnetic tape for further references.

* The Voltage across the capacitor C_T is applied to the inverting input terminal of schmitt trigger A_2 via buffer Amplier A_1.

* The output Voltage swing of the schmitt trigger is designed to Vcc and 0.5 Vcc.

If $R_a = R_b$, ⇒ positive feedback loop.

↓

The Voltage at the non-inverting input terminal of A_2 swings from 0.5 Vcc to 0.25 Vcc.

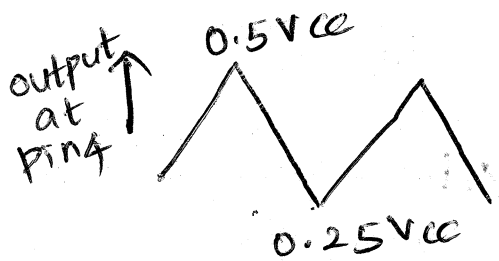
* when the Voltage on the capacitor C_T exceeds 0.5 Vcc during charging, the output of the schmitt trigger goes Low.

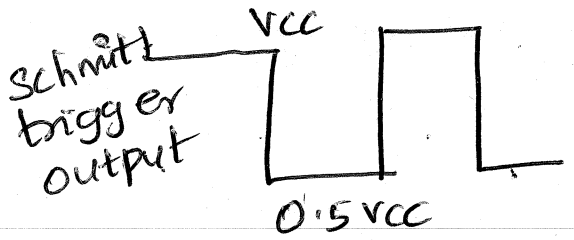
* The capacitor now discharges and when it is at 0.25 Vcc, the output of schmitt trigger goes High.

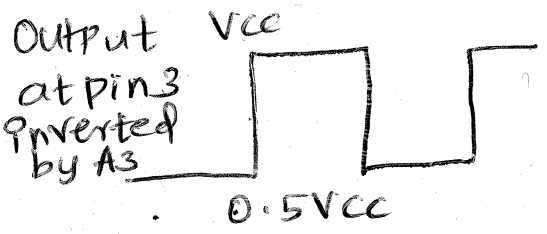
* since the source and sinks current are equal, capacitor charges and discharges for the same amount of time.

* This gives a triangular waveform across C_T which is also available at pin 4.

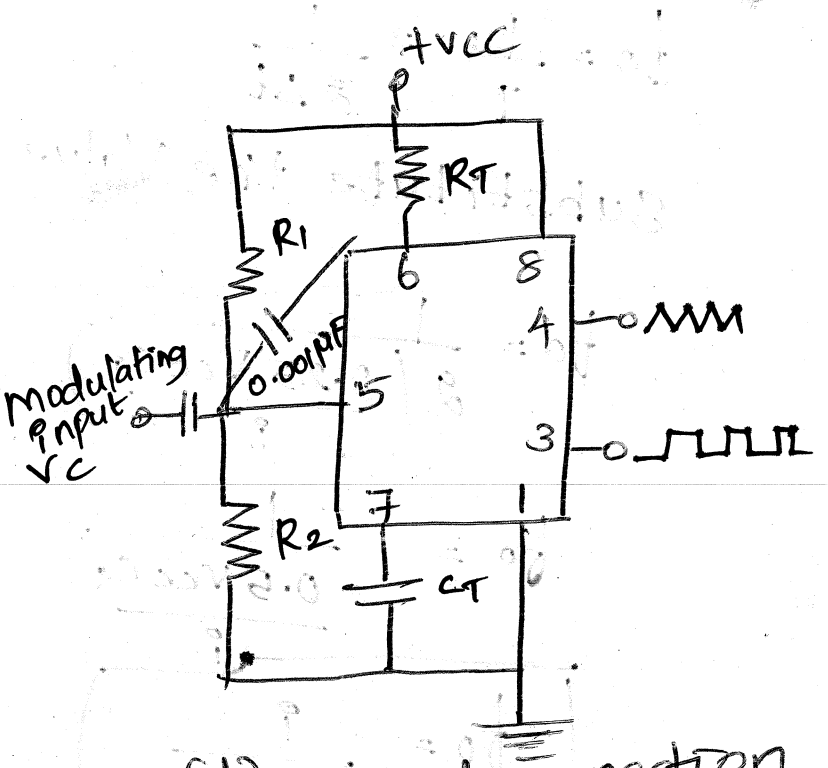
The output frealuency of the Vco can be calculated as follows:







(c) output waveform



(d) Typical connection diagram.

* The total voltage on the capacitor changes from 0.25 Vcc to 0.5 Vcc.
* Thus $\Delta V = 0.25 V_{cc}$.
* The capacitor charges with a constant current source

So,

$$\frac{\Delta V}{\Delta t} = \frac{I}{C_T}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{I}{C_T}$$

$$\Delta t = \frac{0.25 V_{cc} C_T}{I}$$

The time period T of the triangular waveform = $2\Delta t$. The frealuency of oscillator fo is.

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t}$$

Substitute the Value of Δt

$$\therefore f_o = \frac{1}{2\left(\frac{0.25\, V_{cc} C_T}{i}\right)}$$

$$f_o = \frac{1}{\frac{0.5\, V_{cc} C_T}{i}}$$

$$\boxed{f_o = \frac{i}{0.5\, V_{cc} C_T}}$$

We know the Value of i

$$i = \frac{V_{cc} - V_c}{R_T}$$

Substituting the value of i.

$$f_o = \frac{V_{cc} - V_c}{R_T (0.5 V_{cc} C_T)}$$

$$f_o = \frac{V_{cc} - V_c}{0.5 R_T C_T V_{cc}}$$

(or)

$$\boxed{f_o = \frac{2(V_{cc} - V_c)}{V_{cc} R_T C_T}}$$

Note

$$\therefore \frac{1}{0.5} = 2$$

* The output frequency of the VCO can be change either by
  (i) R_T
  (ii) C_T
  (iii) the voltage V_c at the modulating i/p termina
* The voltage V_c can be varied by connecting a R_1 R_2 circuit.
* The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range.
* With no modulating input signal, if the voltage at pin 5 is biased at 7/8 Vcc.

So, $V_c = \frac{7}{8} V_{cc}$

$$f_0 = \frac{2\left(V_{cc} - \left(\frac{7}{8}\right)V_{cc}\right)}{C_T R_T V_{cc}}$$

$$= \frac{2\left(\frac{8V_{cc} - 7V_{cc}}{8}\right)}{C_T R_T V_{cc}}$$

$$= \frac{\cancel{2}\,(8V_{cc} - 7V_{cc})}{\cancel{8_4}(C_T R_T V_{cc})} = \frac{\cancel{V_{cc}}}{4 R_T C_T \cancel{V_{cc}}}$$

$$\boxed{f_0 = \frac{0.25}{R_T C_T}}$$

VOLTAGE TO FREQUENCY CONVERSION FACTOR:

* A parameter of importance for VCO is Voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_o}{\Delta V_c}$$

$\Delta V_c \rightarrow$ modulation voltage required to produce the frequency shift Δf_o for a VCO

$f_o \rightarrow$ original frequency

$f_1 \rightarrow$ new frequency

$$\Delta f_o = f_1 - f_o$$

$$= \frac{2(V_{cc} - V_c + \Delta V_c)}{C_T R_T V_{cc}} - \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}}$$

$$= \frac{2V_{cc} - 2V_c + 2\Delta V_c - 2V_{cc} + 2V_c}{C_T R_T V_{cc}}$$

$$\Delta f_o = \frac{2\Delta V_c}{C_T R_T V_{cc}}$$

$$\Delta V_c = \frac{\Delta f_o C_T R_T V_{cc}}{2}$$

W.K.T $R_T C_T = \frac{1}{4 f_o}$

$$\Delta V_c = \frac{\Delta f_o V_{cc}}{8 f_o}$$

$$8 f_o = \frac{\Delta f_o}{\Delta V_c} V_{cc} \Rightarrow 8 f_o = K_v V_{cc}$$

$$K_v = \frac{8 f_o}{V_{cc}}$$

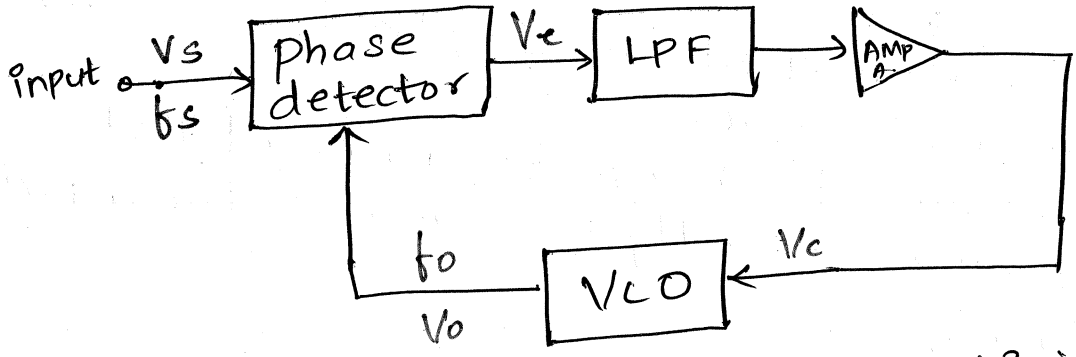
PHASE-LOCKED LOOPS

INTRODUCTION:

* The phase-locked loop is an important building block of linear systems.
* The high cost of realizing PLL in discrete form limited its use earlier.
* PLLs are available inexpensive monolithics ICs.
* This technique for electronic frequency control is used today in satellite communication systems, airborne navigational systems.

BASIC PRINCIPLES:

* The basic block schematic of PLL has be drawn. The feedback system consists of
  1. phase detector / comparator
  2. A Low pass filter
  3. An error amplifier
  4. A Voltage controlled oscillator



* The Vco is a free running multivibrator and operates at a set of frequency fo called free running frequency.
* This frequency is determined by an external timing capacitor and an external resistor.

* It can also be shifted to either side by applying a dc control voltage V_c to an appropriate terminal of IC.
* The frequency deviation is directly proportional to the dc control voltage and hence it is called a voltage controlled oscillator.

* If an input signal V_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V_o of the VCO.

* If the two signals differ in frequency and or phase, an error voltage V_e is generated.
* The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output.
* The high frequency components $(f_s + f_o)$ is removed by the low pass filter and the difference frequency component is amplified and then applied as controlled voltage V_c to VCO.
* The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o.
* once this action starts, we say that the signal is in the capture range.
* The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency.
* The circuit is then said to be locked.
* once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ.

MONOLITHIC PHASE-LOCKED LOOP

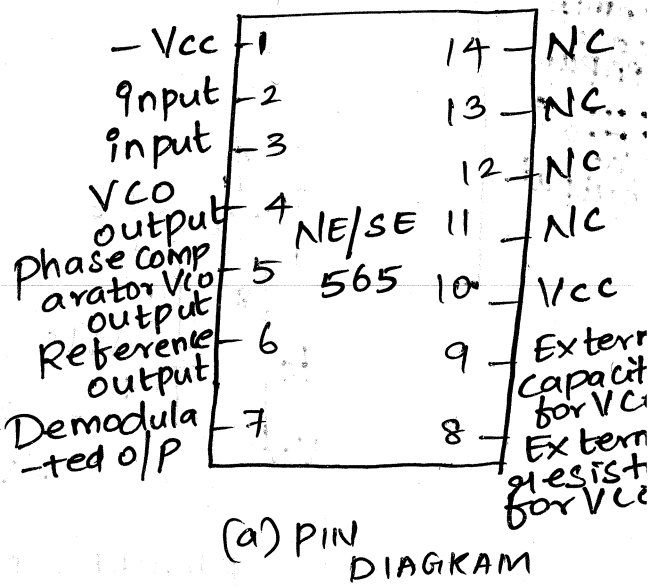
* All the different building blocks of PLL are available as independent IC packages and can be externally inter connected to make a PLL.

IC PLL 565:

* 565 is available as a 14 DIP package.
* The output frequency of the VCO (both inputs 2 and 3 are grounded)

$$f_0 = \frac{0.25}{R_T C_T} \text{ Hz}$$

$R_T \rightarrow$ External Resistor
$C_T \rightarrow$ External capacitor



(a) PIN DIAGRAM

* A Value between 2kΩ and 20kΩ is recommended for R_T.
* The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range.
* It may be seen that phase locked loop is internally broken between the vco output and the phase comparator input.
* A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare fo with input signal fs.
* A capacitor C is connected between pin 7 and pin 10 to make a low pass filter with the internal resistance of 3.6kΩ.

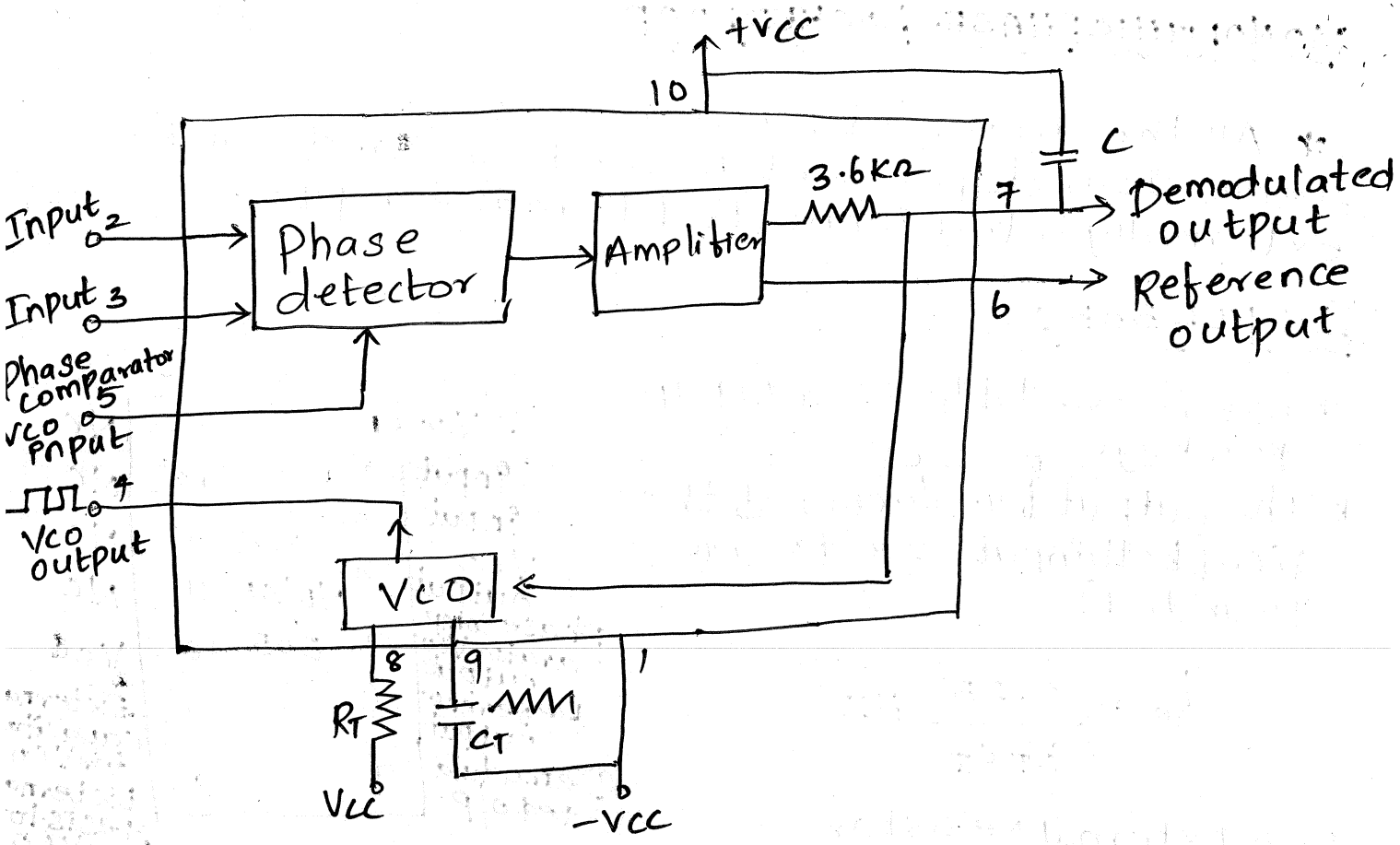


FIGURE: NE/SE565PLL BLOCK DIAGRAM

IMPORTANT ELECTRICAL PARAMETERS OF 565 PLL ARE;

1. Operating frequency range - 0.001 Hz to 500 kHz
2. Operating voltage range - ±6V to ± 12V
3: Input level - 10mV rms min. to 3V
4. output sink current - 1 mA typical
5. Drift in vco centre frequency with temperature - 330 ppm/°C
6. Drift in Vco centre frequency with supply voltage - 1.5 percent/vmax
7. Triangle wave amplitude - 2.4 Vpp at ±6v supply oltag
8. Saluare wave amplitude - 5.4 Vpp at ±6V supply Voltag
9. Bandwidth adjustment range - ± 1 to ± 60%
10. Input impedance - 10 kΩ typical

* This phase difference ϕ generates a corrective control voltage V_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock.
* once locked, PLL tracks the frequency changes of the input signal.
* Thus, a PLL goes through three stages

(i) free running
(ii) capture
(iii) locked (or) tracking

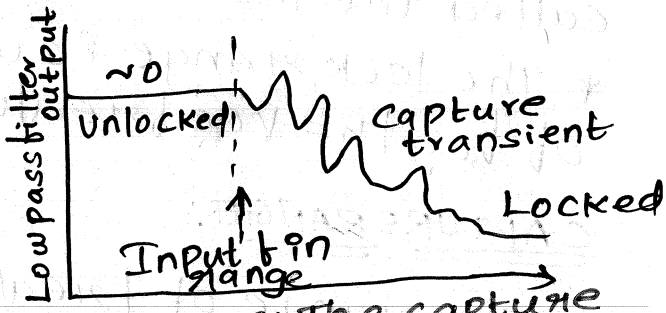


Figure: The capture transient

* It shows the capture transient. As transient capture starts, a small sine wave appears.
* This is due to the difference frequency between the VCO and the input signal.
* The dc component of the beat drives the VCO towards the lock.
* Each successive cycle causes the VCO frequency to move closer to the input signal frequency.
* The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further.
* The process continues until the VCO locks on to the signal and the difference frequency is dc.

* The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond
* we say that the signal is out of the capture band.
* However once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band.
* Thus tracking range is always larger than the capture range.

IMPORTANT DEFINITIONS RELATED TO PLL

LOCK IN RANGE: Once the PLL is locked, it can track frequency changes in the incoming signals.

* The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock in range or tracking range.
* The lock range is usually expressed as percentage of f_o, the VCO frequency.

CAPTURE RANGE:

* The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.
* This parameter is also expressed as percentage of f_o.

PULL-IN TIME:

* The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

DERIVATION OF LOCK-IN RANGE:

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by

$$V_e = K_\phi (\phi - \pi/2) \quad \text{—— (1)}$$

Where

$K_\phi \rightarrow$ phase angle to voltage transfer coefficient of the phase detector.

The control voltage to VCO is

$\therefore V_c = AV_e$

$$V_c = A K_\phi (\phi - \pi/2) \quad \text{—— (2)}$$

$A \rightarrow$ Voltage gain of the amplifier

* This V_c shifts VCO frequency from its free running frequency f_0 to a frequency f given by

$$f = f_0 + K_v V_c \quad \text{—— (3)}$$

$K_v \rightarrow$ Voltage to frequency transfer coefficient of the VCO

* When PLL is locked in to signal frequency f_s then we have

$$f = f_s = f_0 + K_v V_c$$

$$f_s - f_0 = K_v V_c$$

$$V_c = \frac{f_s - f_0}{K_v} \quad \text{—— (4)}$$

Substitute the value of V_c in eqn. (4)

$$A K_\phi (\phi - \pi/2) = \frac{f_s - f_0}{K_v}$$

$$\phi - \frac{\pi}{2} = \frac{f_s - f_0}{A K_v K_\phi}$$

$$\boxed{\phi = \frac{\pi}{2} + \frac{f_s - f_0}{A K_v K_\phi}} \quad \text{——(5)}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian and $V_e(max) = \pm K_\phi \pi/2$

The corresponding value of the maximum control voltage available to drive the VCO will be,

$$V_c(max) = \pm\left(\frac{\pi}{2}\right) K_\phi A \quad \text{—(6)}$$

The maximum VCO frequency swing that can be obtained is given by

$$(f - f_0)_{max} = K_v V_c(max)$$

→ Substitute the value of $V_c(max)$

$$= K_v \left(\frac{\pi}{2}\right) K_\phi A$$

$$\boxed{(f - f_0)_{max} = \frac{\pi}{2} K_v K_\phi A} \quad \text{— (7)}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be

$$f_s = f_0 \pm (f - f_0)_{max}$$

Sub. the $(f - f_0)_{max}$ value

$$= f_0 \pm \frac{\pi}{2} K_v K_\phi A$$

$$\boxed{f_s = f_0 \pm 2\Delta f_L} \quad \text{— (8)}$$

considering $2\Delta f_L = \pi K_v K_\phi A$

where 2 Δf_L will be the lock in frequency range and is given by

$$\text{Lock in range} = 2\Delta f_L = K_v K_\phi A \pi$$

$$\Delta f_L = K_v K_\phi A \frac{\pi}{2}$$

The Lock-in range is symmetrically located with respect to VCO free running frequency f_o.

For IC PLL 565

$$K_v = \frac{8 f_o}{V}$$

where, $V = +V_{cc} - (-V_{cc})$

$$K_\phi = \frac{1.4}{\pi}$$

$\therefore A = 1.4$

Hence the Lock in range will becomes

$$\Delta f_L = \pm K_v K_\phi A (\pi/2)$$

$$= \pm \frac{8 f_o}{V} \times \frac{1.4}{\pi} \times 1.4 \times \frac{\pi}{2}$$

$$= \pm 4 \times 1.96 \frac{f_o}{V}$$

$$\boxed{\Delta f_L = \pm \frac{7.8 f_o}{V}}$$

On substituting those values we get the final value of Δf_L.

DERIVATION OF CAPTURE RANGE:

* Initially, when PLL is not locked to the signal the frequency of the VCO will be free running frequency f_0.
* The phase angle difference between the signal and the VCO output. Voltage will be

$$\phi = (\omega_s t + \theta_s) - (\omega_0 t + \theta_0)$$

$$= \omega_s t + \theta_s - \omega_0 t - \theta_0$$

$$\phi = (\omega_s - \omega_0) t + \Delta\theta \quad \text{—— (1)}$$

$\therefore \Delta\theta = \theta_s - \theta_0$

Thus by the phase angle difference does not remain constant but will change with time at a rate given by:

$$\frac{d\phi}{dt} = \omega_s - \omega_0 \quad \text{—— (2)}$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_0) = \Delta f$

The Low pass filter is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} \quad \text{—— (3)}$$

Where $f_1 = \frac{1}{2\pi RC}$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) \cong \frac{f}{\partial f} \quad \text{—— (4)}$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency

$$\Delta f = fs - fo.$$

if $\Delta f > 3f_1$, the LPF transfer function will be approximately,

(Sub the value of Δf)

$$T(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{fs - fo} \quad \text{—— (5)}$$

The voltage V_c to drive the VCO is

$$V_C = Ve \times T(f) \times A$$

(or)

$$V_c(max) = Ve(max) \times T(f) \times A \quad \text{—— (6)}$$

W.K.T

$$\rightarrow Ve(max) = K\phi(\pi/2)$$

$$\rightarrow T(f) = \frac{f_1}{\Delta f}$$

$$V_c(max) = \pm K\phi(\pi/2) A (f_1/\Delta f)$$

Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_0)_{max} = K_V V_c(max)$$

$$= K_V K\phi(\pi/2) A (f_1/\Delta f) \quad \text{—— (7)}$$

For the acquisition of signal frequency, we should put $f = f_s$,

So that the maximum signal frequency range that can be acquired by PLL is

$$(f_s - f_0)_{max} = \pm K_v K_\phi (\pi/2) A \; (f_1/\Delta f_L)$$

$$\Delta f = (f_s - f_0)_{max}$$

$$\Delta f = \pm K_v K_\phi (\pi/2) A \frac{f_1}{\Delta f}$$

$$(\Delta f)^2 = \pm K_v K_\phi \left(\frac{\pi}{2}\right) A f_1$$

Since $\Delta f_L = \pm K_v K_\phi (\pi/2) A$

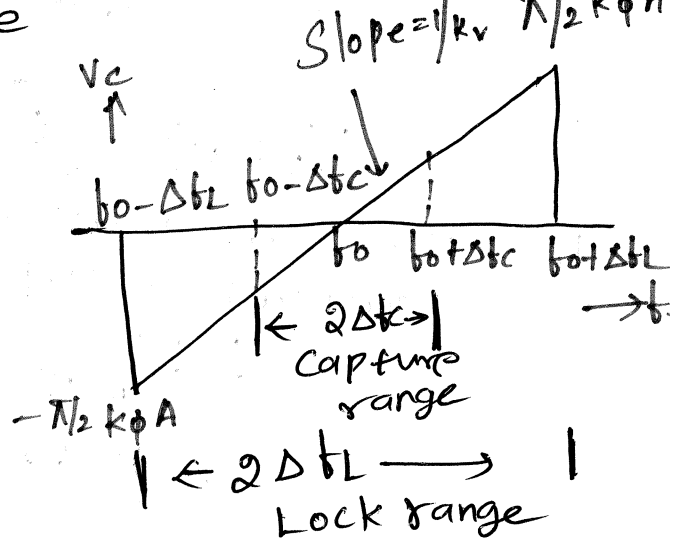
$$(\Delta f)^2 = \pm f_1 \Delta f_L$$

$$\Delta f = \pm \sqrt{f_1 \Delta f_L}$$

∴ Therefore, the total capture range is

$$\boxed{2\Delta f_c \simeq 2\sqrt{f_1 \Delta f_L}}$$

* In order to increase the ability of lock in range, large capture range is required
* However, a large capture range will make the PLL more susceptible to noise and undesirable signal



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PLL APPLICATIONS:

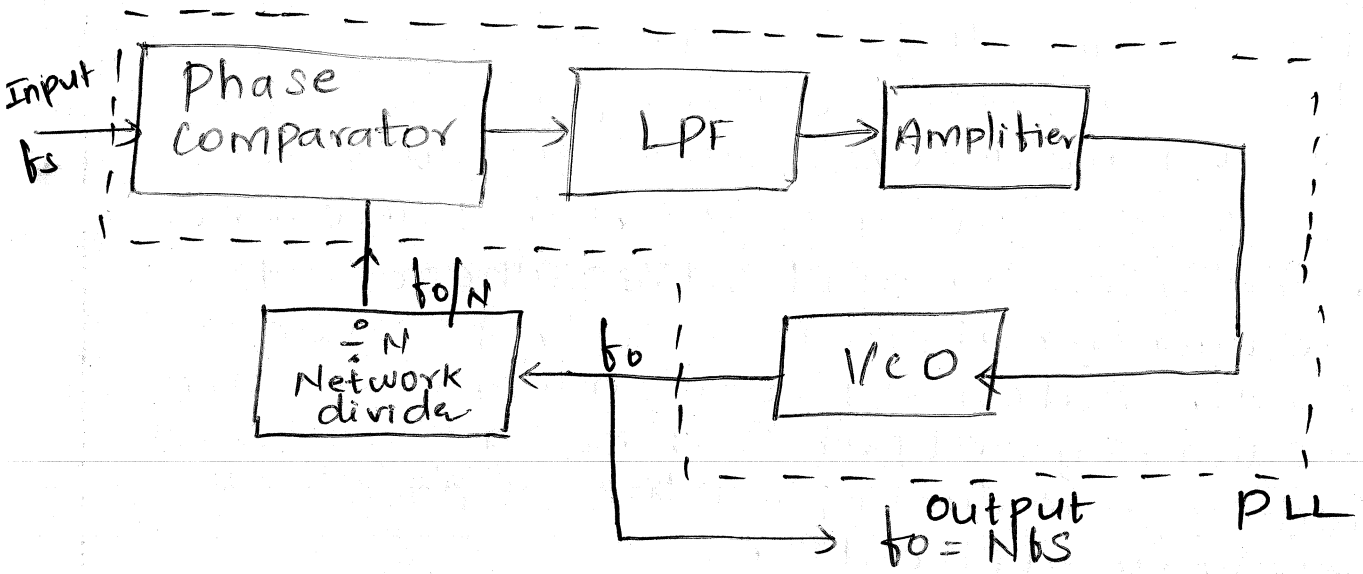
* The Output from a PLL system can be obtained either as the Voltage signal $V_c(t)$ corresponding to the error Voltage in the feedback loop, or as a frequency signal at VCO output terminal.
* The Voltage output is used in frequency discrimination application whereas the frequency output is used in frequency discrimination application where as the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

* Consider the case of Voltage output. When PLL is locked to an input frequency, the error Voltage $V_c(t)$ is proportional to $(f_s - f_0)$.

* If the input frequency is varied as in the case of FM signal, V_c will also vary in order to maintain the lock.
* Thus the Voltage output serves as a frequency discriminator which converts the input frequency changes to Voltage changes.

* In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input.

FREQUENCY MULTIPLICATION/DIVISION



* It shows the block diagram of a frequency multiplier.
* A divide by N network is inserted between the VCO output and the phase comparator input.
* In the locked state, the Vco output frequency fo is given by

$$f_o = N f_s$$

* The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.
* Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.
* If the input signal is rich in harmonics, then Vco can be directly locked to the nth harmonic of the input signal without connecting any frequency divider in between

* However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n.
* Typically n is kept less than 10.
* Since the Vco output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the Vco output with the input signal fs.
* The output fo of Vco is now given by

$$f_o = \frac{f_s}{m}$$

FREQUENCY TRANSLATION:

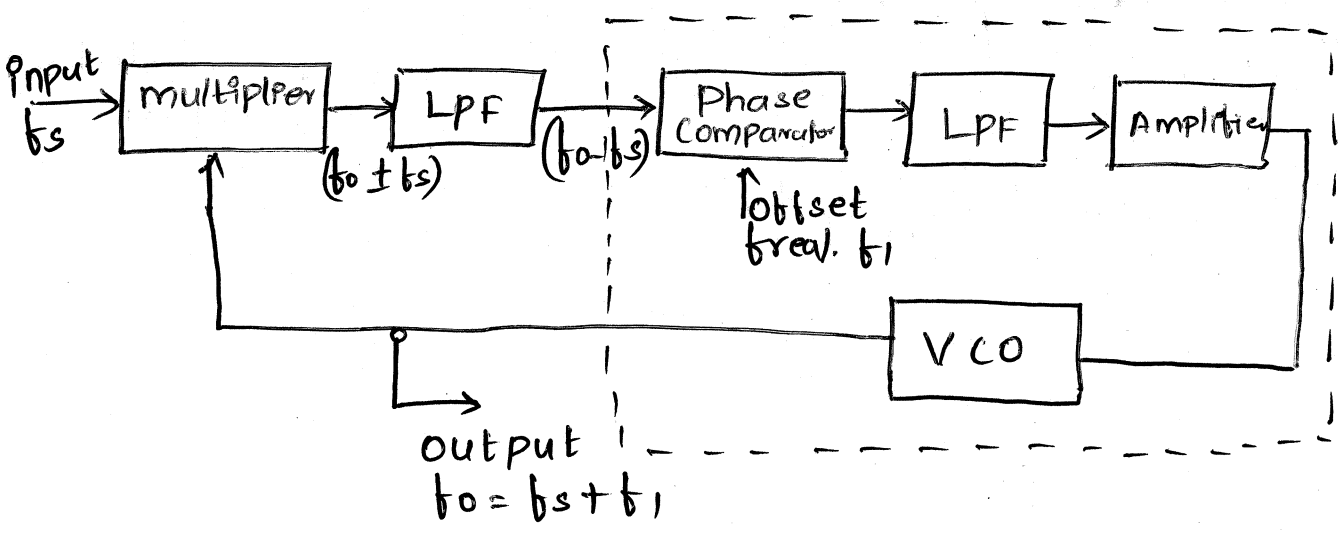


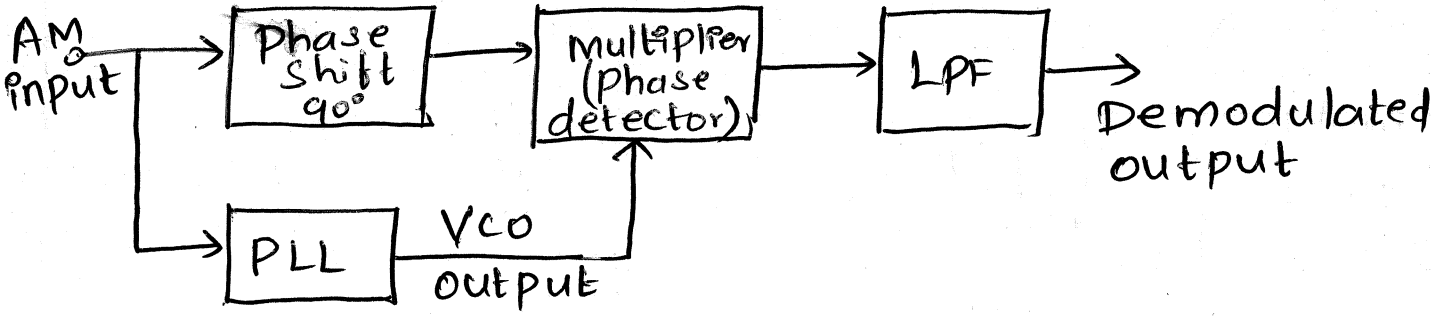
FIGURE: PLL used as a frequency translator

* A schematic for shifting the frequency of an oscillator by a small factor is shown in this diagram.
* It can be seen that a mixer and a low pass filter are connected externally to the PLL.

* The signal fs which has to be shifted and the output frequency fo of the VCO are applied as inputs to the mixer.
* The output of the mixer contains the sum and difference of fs and fo.
* However, the output of LPF contains only the difference signal (fo - fs).
* When PLL is in locked state,

$$f_o - f_s = f_1$$
$$f_o = f_s + f_1$$

AM DETECTION:



* A PLL may be used to demodulate AM signals as shown in figure.
* The PLL is locked to the carrier frequency of the incoming AM signal.
* The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier.
* since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to

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* This makes both the signals applied to the multiplier in the same phase.
* The output of the multiplier contains both the sum and difference signals, the demodulated output is obtained after filtering high frequency components by the LPF.
* since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

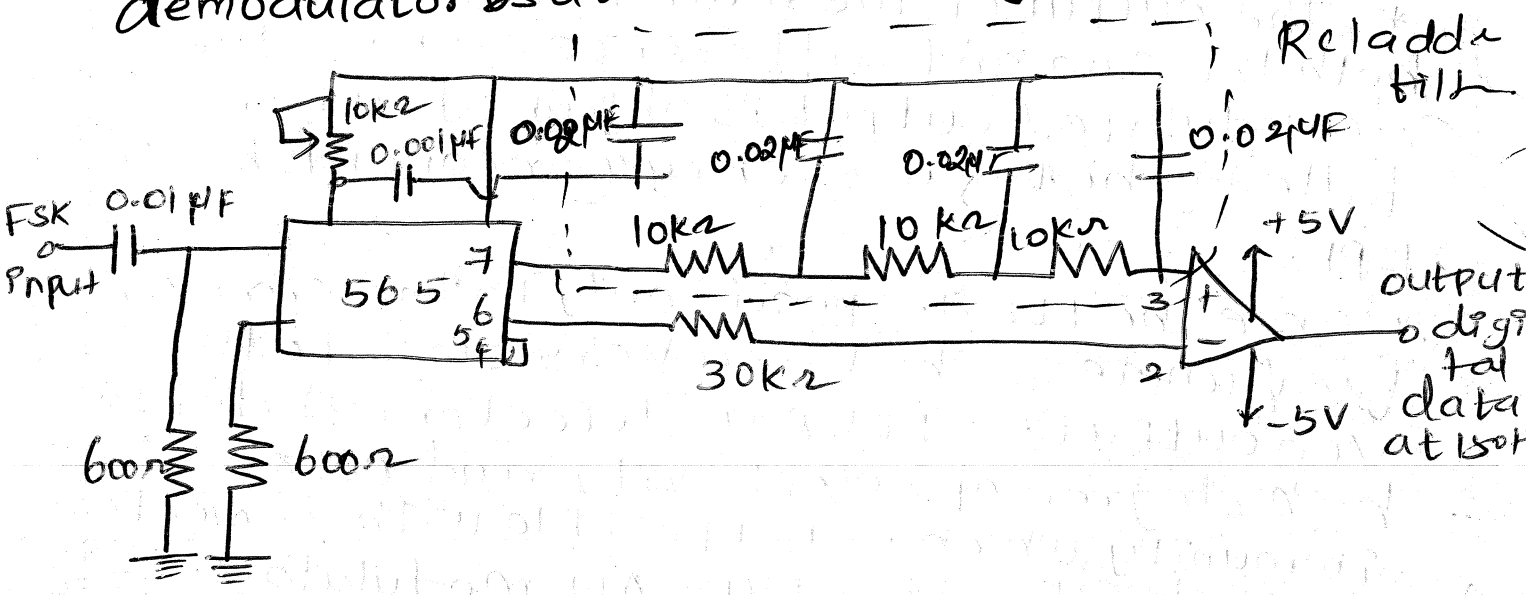
FM DEMODULATION:

* If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal.
* The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.
* The VCO transfer characteristics determine the linearity of the demodulated output.
* since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

FREQUENCY SHIFT KEYING DEMODULATOR:

* In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies.

* This type of data transmission is called frequency shift keying technique.
* The binary data can be retrived using a FSK demodulator at the receiving end.



(a) FSK demodulator

* The 565 PLL is very useful as a FSK demodulator
* The Figure shows FSK demodulator using PLL for tele-typewriter signals of 1070Hz and 1270Hz.
* As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.
* A three stage filter removes the carrier component and the output signal is made logic compatible by a Voltage Comparator.

(18) ×2 = (20) copies