IInd YEAR

EE8451

LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

UNIT-III

APPLICATIONS OF OP-AMP

INSTRUMENTATION AMPLIFIER:

* In a number of industrial and consumer applications, one is required to measure and control physical quantities.
* Some typical examples are measurement and control of temperature, humidity, light intensity.
* These quantities are measured with the help of transducers
* The output of transducer has to be amplified so that it can drive the indicator or display system.

FEATURES OF INSTRUMENTATION AMPLIFIER:

* high gain accuracy
* high CMRR
* high gain stability with low temperature coefficient
* low dc offset
* Low output impedance.

$$V_o = -\frac{R_2}{R_1} V_2 + \frac{1}{1+\frac{R_3}{R_4}} V_1 \left(1+\frac{R_2}{R_1}\right)$$

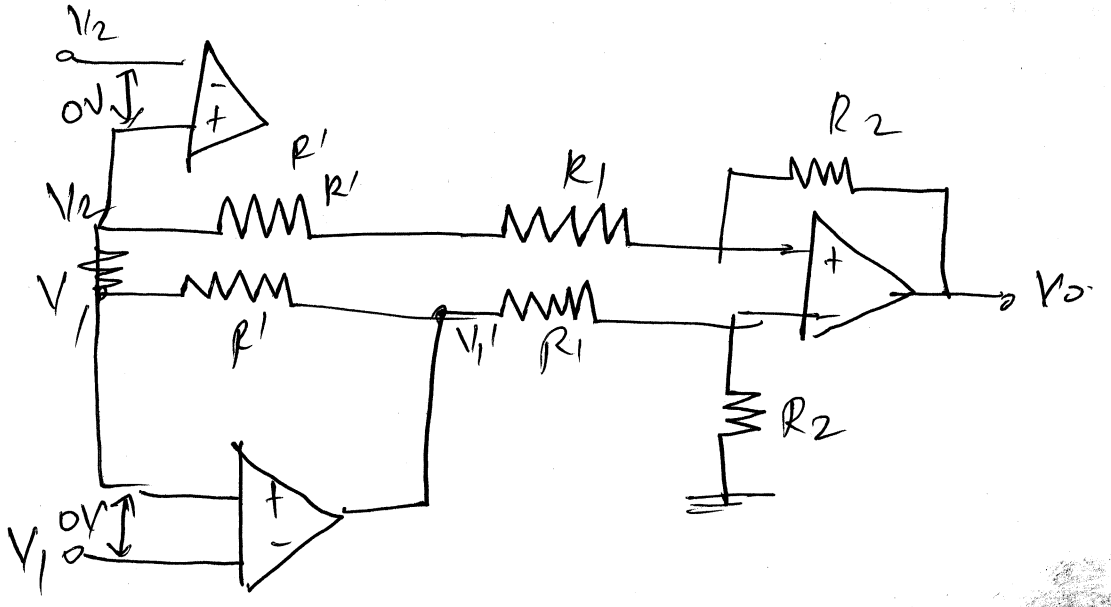
$$V_o = \frac{-R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}} \left(\frac{R_1}{R_1}+1\right) V_1 \right]$$

For $\frac{R_1}{R_2} = \frac{R_3}{R_4}$ $\quad V_o = \frac{R_2}{R_1}(V_1 - V_2)$

* The op-amps A_1 and A_2 have differential input voltage as zero.
* For $V_1 = V_2$, that is under commonmode operation the voltage across R will be zero.
* As no current flows through R and R' the noninverting amplifier A_1 acts as voltage follower.
* So its output $V_2' = V_2$.
* Similarly op-amp A_2 acts as voltage follower having output $V_1' = V_1$.
* If $V_1 \neq V_2$, current flows in R and R' and $(V_2' - V_1') > (V_2 - V_1)$
* Therefore this circuit has differential gain and CMRR more compared.

$$V_o = -\frac{R_2}{R_1} V_2' + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1 + R_2}\right)$$

$$= \frac{R_2}{R_1}\left(V_1' - V_2'\right)$$



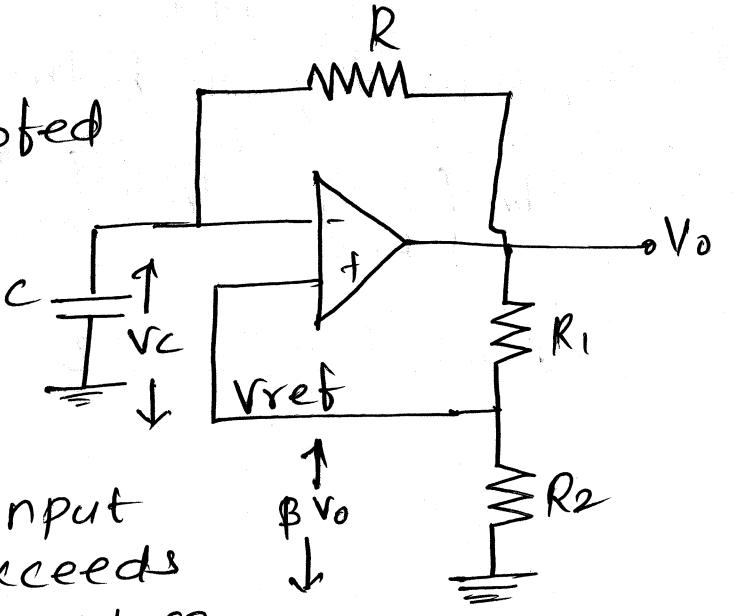
SQUARE WAVE GENERATORS:

* Besides generating sine waves, the op-amp generates saluare waveform and pulses, an active device generate a saluare waveform is also called as multivibrator

(i) Astable multivibrator

* It is also called as free running oscillator, the principle of generation of saluare wave output is to force an op-amp to operate in the saturation region.

$$\beta = \frac{R_2}{R_1 + R_2}$$



* The output is also fed back to inverting terminal input after integrating by lowpass RC combination.
* Whenever the input at (-) input just exceeds Vref switching takes place to +Vsat to −Vsat.

$$V_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

$V_f = +V_{sat}$

$V_i = -\beta V_{sat}$

considering

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC}$$

at $t = T_1$

$$V_c(t) = +\beta V_{sat}$$

$$\beta V_{sat} = V_{sat} - (\beta V_{sat} + V_{sat}) e^{-T_1/RC}$$

$$\beta V_{sat} - V_{sat} = -V_{sat}(1+\beta) e^{-T_1/RC}$$

$$V_{sat}(\beta - 1) = -V_{sat}(1+\beta) e^{-T_1/RC}$$

$$V_{sat}(1-\beta) = V_{sat}(1+\beta) e^{-T_1/RC}$$

$$e^{-T_1/RC} = \frac{1-\beta}{1+\beta}$$

Taking log on both sides

$$\ln\left(\frac{-T_1}{RC}\right) = \ln\left(\frac{1-\beta}{1+\beta}\right)$$

Considering $\beta = 0.5$

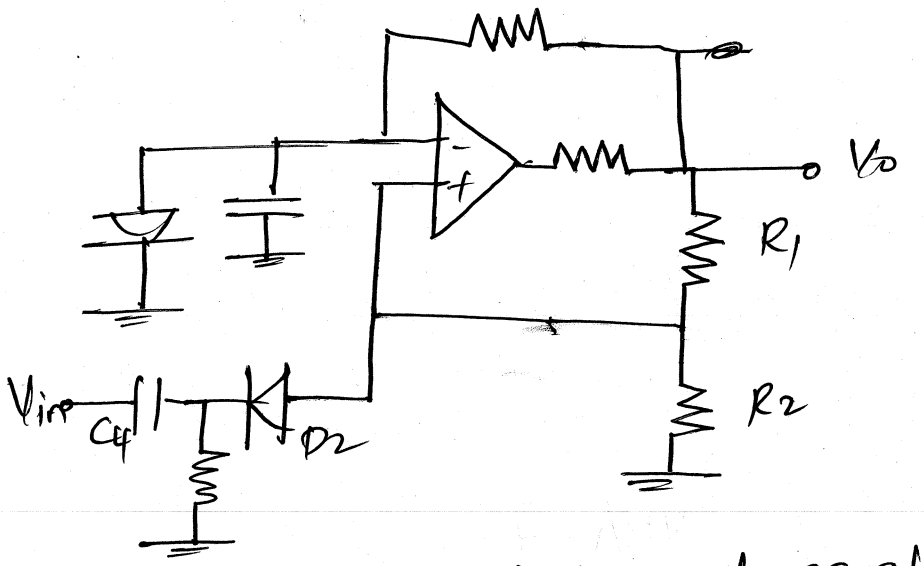
$$\frac{-T_1}{RC} = \ln\left(\frac{1-0.5}{1+0.5}\right)$$

$$\frac{-T_1}{RC} = \ln\left(\frac{0.5}{1.5}\right)$$

$$\frac{-T_1}{RC} = \ln\left(\frac{1}{3}\right)$$

$$\boxed{T_1 = 1.1\,RC}$$

(ii) MONOSTABLE MULTIVIBRATOR:



* It has one stable state and one aluasi stable state.
* This circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal.
* The width of output signal depends only on external components connected to the op-amp
* Diode D_1 clamps the capacitor voltage to 0.7V when output is $+V_{sat}$.
* A negative going pulse signal of magnitude V_i passing through differentiator R_4 C_4 and diode D_2 produces going triggering impulse and is applied to the (+) input terminal.

$$V_o = V_f + (V_i - V_f) e^{-t/RC}$$

$$V_f = -V_{sat}$$

$$V_i = V_D$$

$$V_o = -V_{sat} + (V_D + V_{sat}) e^{-t/RC}$$

At $t = T$, $V_o = -\beta V_{sat}$

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat}) e^{-T/RC}$$

$$-\beta V_{sat} + V_{sat} = (V_D + V_{sat}) e^{-T/RC}$$

$$\frac{V_{sat}(1-\beta)}{V_D + V_{sat}} = e^{-T/RC}$$

$$\frac{V_{sat}(1-\beta)}{V_{sat}\left(1 + \frac{V_D}{V_{sat}}\right)} = e^{-T/RC}$$

$$-\frac{T}{RC} = \ln\left(\frac{1 + V_D/V_{sat}}{1-\beta}\right)$$

$$T = RC \ln(1-\beta)$$

$V_{sat} >> V_D$

$R_1 = R_2$

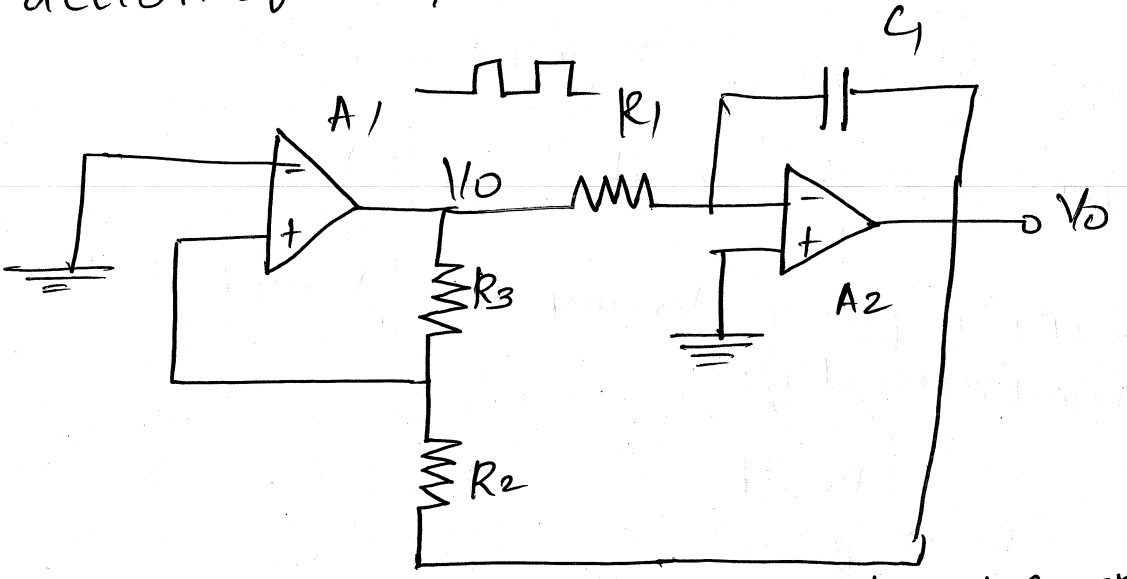
$\beta = 0.5$

$$\boxed{T = 0.69\,RC}$$

* Monostable multivibrator circuit is also referred as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger

TRIANGULAR WAVE GENERATOR:

* Generally triangular wave generator may be derived from other sources through the use of comparators.
* Linear wave forms such as triangle and ramps may be derived from the charge/discharge action of a capacitor.



* It basically consists of two level comparator followed by integrator circuit. The output of A_1 is a saluare wave of amplitude $\pm V_{sat}$ and is applied to the (-) i/p of the integrator producing a triangular wave.

$$P = V_f + (V_i - V_f)\beta$$

$$V_f = -V_{ramp}$$

$$V_i = +V_{sat}$$

$$\beta = \frac{R_2}{R_2 + R_3}$$

$$P = -V_{ramp} + (V_{sat} + V_{ramp})\frac{R_2}{R_2 + R_3}$$

At; $t = t_1$; Voltage at p becomes equal to zero

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat}) \quad \text{—— (1)}$$

at $t = t_2$, when output of A_1 switches from $-V_{sat}$ to $+V_{sat}$

$$V_{ramp} = -\frac{R_2}{R_3}(-V_{sat}) \quad \text{—— (2)}$$

peak to peak value of output is

$$V_o(PP) = +V_{ramp} - (-V_{ramp})$$

$$V_o(PP) = 2\frac{R_2}{R_3}V_{sat} \quad \text{—— (3)}$$

The output from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$

$$V_o = \frac{-1}{RC}\int V_i\,dt$$

$$V_o(PP) = \frac{-1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt$$

$$= \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

$$T = 2R_1C_1\frac{V_o(PP)}{V_{sat}} \quad \text{—— (4)}$$

putting $V_o(PP)$ value

$$T = 2R_1C_1\frac{2\frac{R_2}{R_3}V_{sat}}{V_{sat}}$$

$$= \frac{4R_1C_1R_2}{R_3}$$

$$\boxed{f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}}$$

WRITE IN DETAIL ABOUT ANALOG MULTIPLIER AND ITS APPLICATIONS?

* Transistors and operational amplifiers used to design Analog multiplier ICs.
* A Multiplier produces an output V_o which is proportional to the product of two inputs V_x and V_y.
* Quadrant defines the applicability of the circuit of bipolar signs at the inputs

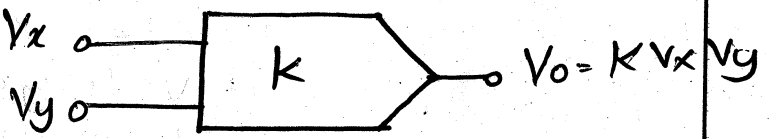


FIG: MULTIPLIER SYMBOL

First Quadrant → only positive input signals
Two Quadrants → one bipolar and one unipolar signal
Four Quadrants → Two Bipolar signal.

Multiplier performance is specified in terms of accuracy and non-linearity.

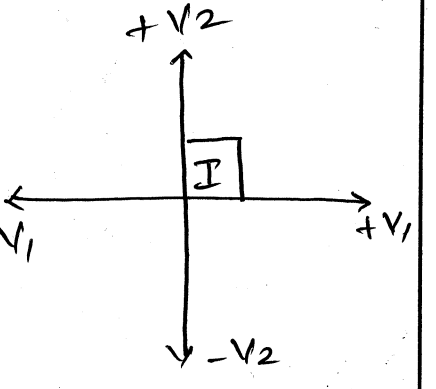
Accuracy: Represents the maximum deviation of the actual output from the ideal value. This deviation also referred to as Total error.

Non-linearity: * Also referred as linearity error.
* maximum output deviation from the best straight for the case where one i/p is varied from one end to end and other end is kept fixed.

MULTIPLIER MODES OF OPERATION:

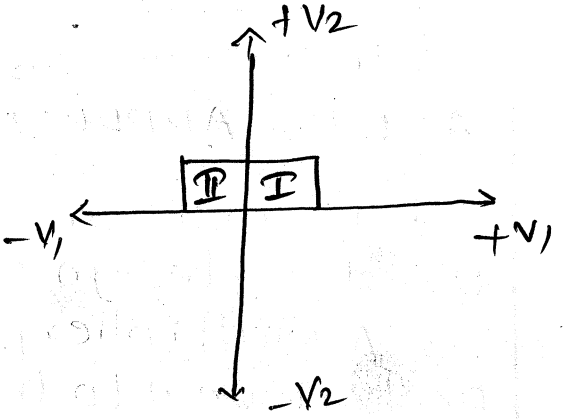
(i) one quadrant multiplier:

* In this modes of operation of a multiplier, both the input signal V_1 and V_2 are positive polarity.



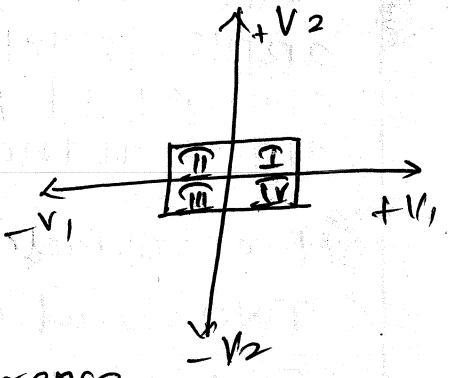
(ii) Two quadrant multiplier:

* In this mode of operation of a multiplier one of the input V_1 (or) V_2 held positive, and another input allowed to swing both positive and negative.



(iii) Four quandrant multiplier:

* In this mode of operation both the input voltages V_1 and V_2 swings both positive and negative



FEATURES:

* High input impedance
* Laser trimmed 10V scaling reference
* No external components required
* Supply voltage ranging from +8V to +18V

APPLICATIONS:

(i) FREQUENCY DOUBLER

Let $V_1 = V_x \sin\omega t$

$V_2 = V_y \sin\omega t$

Generally multiplier output

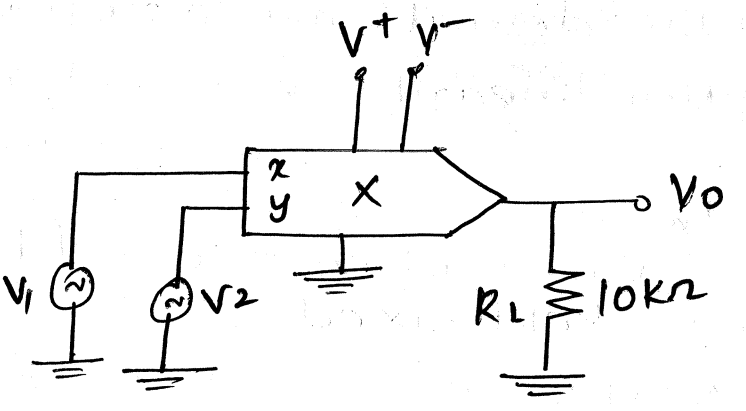
$$V_o = \frac{V_1 V_2}{V_{ref}}$$

$$V_o = \frac{V_x V_y \sin^2\omega t}{V_{ref}}$$

$\because \sin^2\theta = \frac{1-\cos 2\theta}{2}$

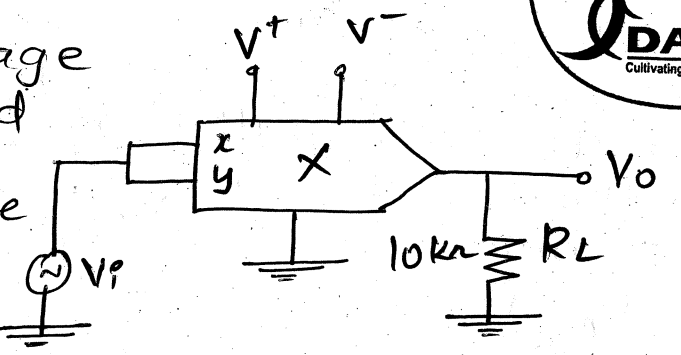
$$V_o = \frac{V_x V_y}{V_{ref}}\left(\frac{1-\cos 2\omega t}{2}\right)$$

$$V_o = \frac{V_x V_y}{2V_{ref}} - \frac{V_x V_y \cos 2\omega t}{2V_{ref}}$$



* The output contai a dc term and negative cosine wave of double frequen The dc term can be easil removed by using 1μF coupling capacitor b/w load and o/p termina

(ii) VOLTAGE SQUARER



* Let sine wave voltage $V_i = V_m \sin \omega t$ applied on both the inputs then the output voltage V_o.

$$V_o = \frac{V_i^2}{V_{ref}}$$

$$K = \frac{V_o}{V_i^2} \text{ (or) } V_o = K V_i^2$$

example:

$V_i = 5 \sin 2\pi 10^4 t$

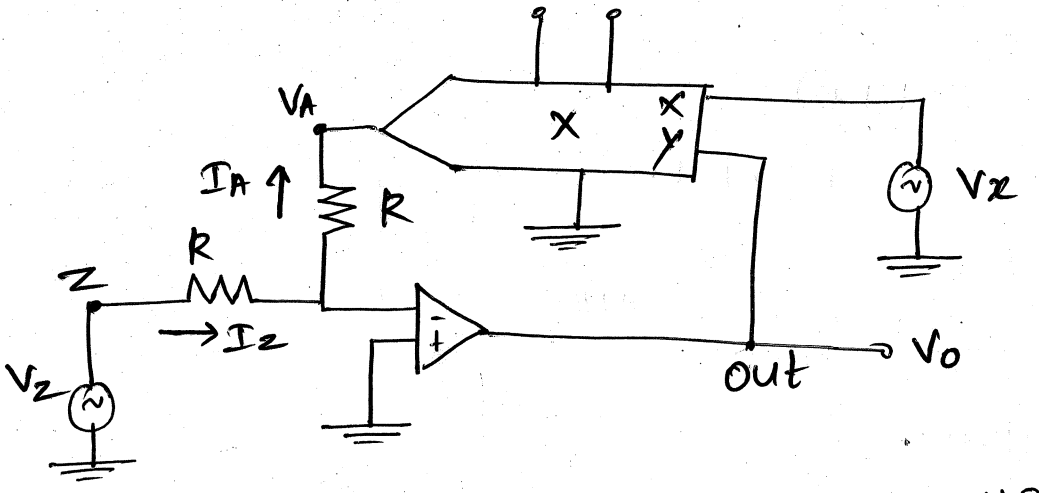
$V_{ref} = 10\,V$

$$V_o = \frac{5^2 (\sin 2\pi \times 10^4 t)^2}{10}$$

$$= 2.5 \left(\frac{1}{2} - \frac{1}{2} \cos 2\pi \times 2 \times 10^4 t \right)$$

$$= 1.25 - 1.25 \cos 2\pi \times 2 \times 10^4 t$$

(iii) VOLTAGE DIVIDER:



* Division is the complement of multiplication can be design by placing the multiplier circuit element in the op-amp feed back loop.

The output voltage V_A of the amplifier.

$$V_A = \frac{V_x V_y}{V_{ref}} = \frac{V_x V_o}{V_{ref}}$$

$$V_A = -I_A R$$

$$I_A = -\frac{V_A}{R}, \quad I_A = -\frac{V_x V_o}{R V_{ref}}$$

$$\therefore I_z = I_A$$

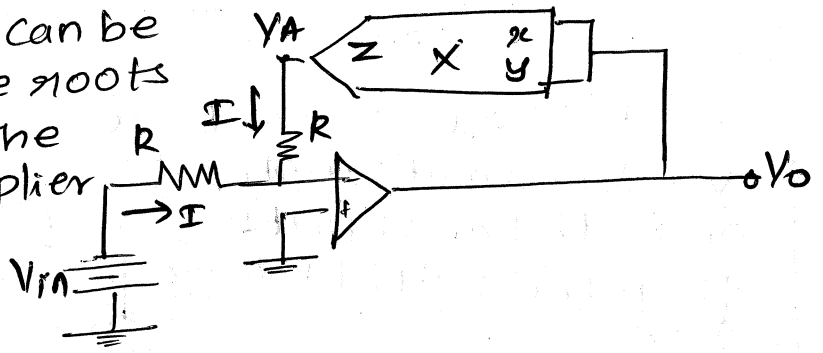
$$I_z = \frac{-V_x V_o}{V_{ref} R}$$

$$V_z = I_z R = -\frac{V_x V_o}{V_{ref} R}$$

$$V_o = -V_{ref} \frac{V_z}{V_x}$$

(iv) SQUARE ROOTER:

* A divider circuit can be used to find saluare roots by connecting both the inputs of the multiplier to the output of an op-amp.



$$V_A = \frac{V_o^2}{V_{ref}}$$

$$V_A = -V_{in}$$

$$-V_{in} = \frac{V_o^2}{V_{ref}}$$

$$V_o^2 = -V_{in} V_{ref}$$

$$V_o = \sqrt{V_{in} V_{ref}}$$

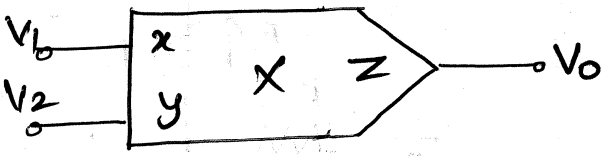
* Thus the output voltage is saluare rooter by connecting both the inputs of the multiplier.

(v) PHASE ANGLE DETECTION:

$$V_1 = V_x \sin \omega t$$

$$V_2 = V_y \sin(\omega t + \theta)$$

$$V_o = \frac{V_x V_y}{V_{ref}} \sin \omega t \sin(\omega t + \theta)$$



$$\sin A \sin B = \frac{1}{2}[\cos(A-B) - \cos(A+B)]$$

$$= \frac{1}{2}[\cos(\omega t - \omega t - \theta) - \cos(\omega t + \omega t + \theta)]$$

$$= \frac{1}{2}[\cos(-\theta) - \cos(2\omega t + \theta)]$$

$$= \frac{1}{2}[\cos\theta - \cos(2\omega t + \theta)]$$

The dc term in the output is $V_o = \frac{V_x V_y}{V_{ref}} \frac{1}{2} \cos\theta$

The output voltage proportional to phase difference θ.

EXPLAIN IN DETAIL ABOUT ANALOG MULTIPLIER USING EMITTER COUPLED TRANSISTOR PAIR:

* simple modulator using differential amplifier
* It can be used as a multiplier
* It has two transistor Q1 and Q2 act as a differential amplifier.
* input V1 is given to differential amplifier ckt.
* The input signal V2 is given to emitter coupled differential pair through constant current source.
* This multiplier circuit provides the output at two quadrant only.

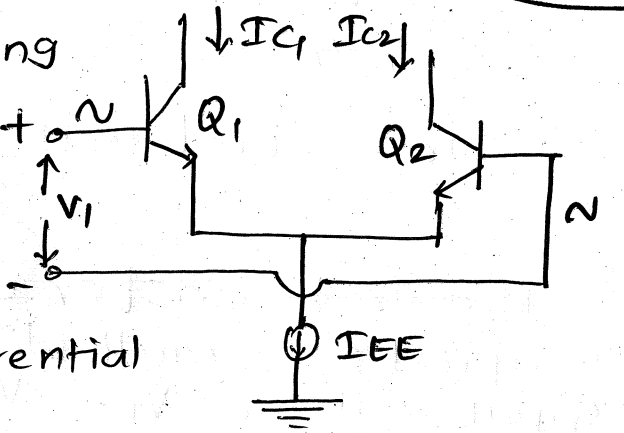


FIG: EMITTER COUPLED TRANSISTOR PAIR

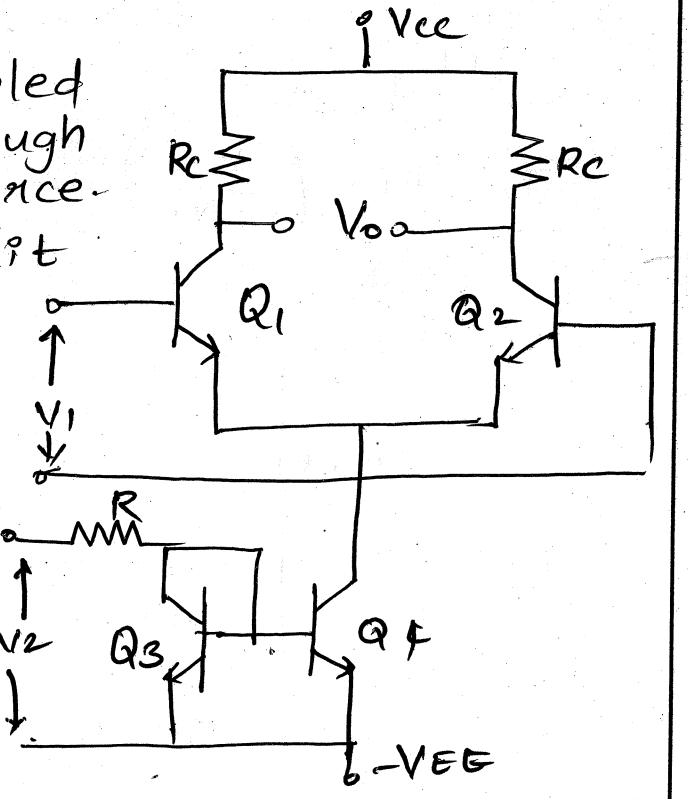


FIG: SIMPLE MODULATOR TYPE MULTIPLIER

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_1/V_T}}$$

$$I_{C2} = \frac{I_{EE}}{1 + e^{V_1/V_T}}$$

$V_T \Rightarrow$ Thermal voltage

$$\Delta I_C = I_{C1} - I_{C2}$$

$$= \frac{I_{EE}}{1 + e^{V_1/V_T}} - \frac{I_{EE}}{1 + e^{V_1/V_T}}$$

$$= I_{EE}\left[\frac{1}{1 + e^{-V_1/V_T}} - \frac{1}{1 + e^{V_1/V_T}}\right]$$

Note: $\frac{1}{1+e^{-x}} - \frac{1}{1+e^{x}} = \tanh\left(\frac{x}{2}\right)$

$\therefore x = \frac{V_1}{V_T}$

$$\Delta I_C = I_{EE} \tanh \frac{V_1}{2V_T}$$

The dc transfer characteristics of emitter coupled pair multiplier. when the differential input voltage $V_1 << V_T$

$$\Delta I_C = I_{EE} \tanh\left(\frac{V_1}{2V_T}\right)$$

$$= I_{EE}\left(\frac{V_1}{2V_T}\right)$$

$$\Delta I_C = I_{EE}\left(\frac{V_1}{2V_T}\right)$$

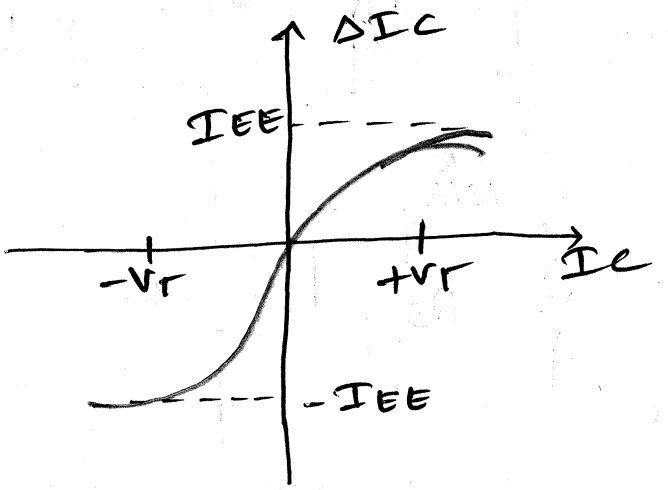


FIG: TRANSFER CHARACTERISTICS

GILBERT MULTIPLIER CELL:

* The Gilbert multiplier cell is a modification of the emittercoupled cell and allow this four quadrant multiplication.

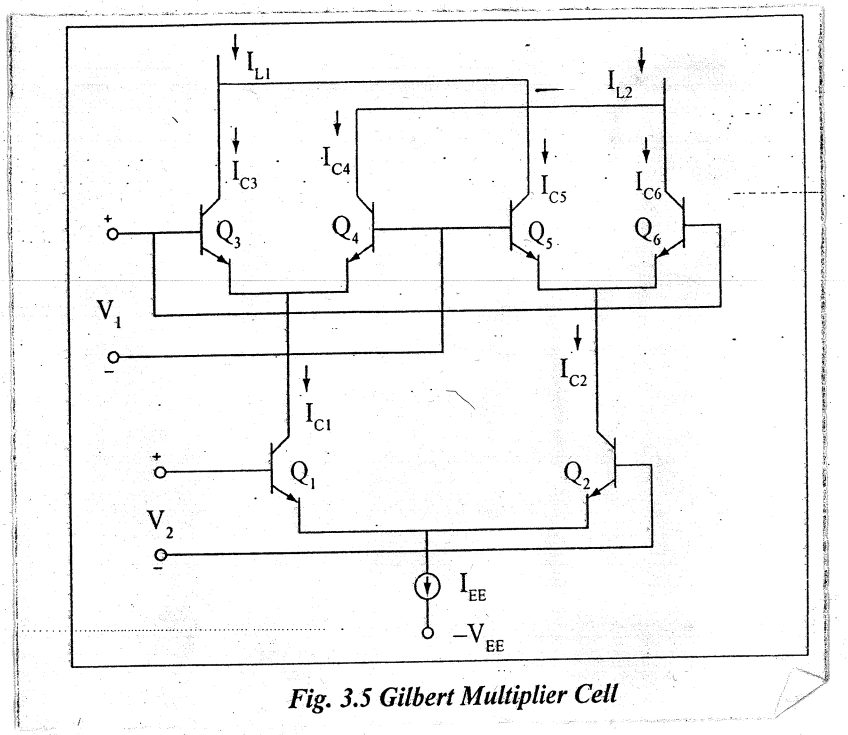


Fig. 3.5 Gilbert Multiplier Cell

ANALYSIS:

$$I_{C3} = \frac{I_{C1}}{1+e^{-V_1/V_T}}, \quad I_{C4} = \frac{I_{C1}}{1+e^{V_1/V_T}} \quad \text{---(1)}$$

$$I_{C5} = \frac{I_{C2}}{1+e^{V_1/V_T}}; \quad I_{C6} = \frac{I_{C2}}{1+e^{-V_1/V_T}} \quad \text{---(2)}$$

The collector currents I_{C_1} and I_{C_2}

$$I_{C_1} = \frac{I_{EE}}{1+e^{-V_2/V_T}}$$

$$I_{C_2} = \frac{I_{EE}}{1+e^{V_2/V_T}}$$

Substitute I_{C1} in I_{C3} and I_{C4}

$$I_{C3} = \frac{I_{EE}}{\left(1+e^{-V_1/V_T}\right)\left(1+e^{-V_2/V_T}\right)}$$

$$I_{C4} = \frac{I_{EE}}{\left(1+e^{V_1/V_T}\right)\left(1+e^{-V_2/V_T}\right)}$$

Substitute I_{C2} in I_{C5} and I_{C6}

$$I_{C5} = \frac{I_{EE}}{\left(1+e^{+V_1/V_T}\right)\left(1+e^{V_2/V_T}\right)}$$

$$I_{C6} = \frac{I_{EE}}{\left(1+e^{V_2/V_T}\right)\left(1+e^{-V_1/V_T}\right)}$$

The differential output current $\Delta I = I_{L1} - I_{L2}$

$I_{L1} = I_{C3} + I_{C5}$; $I_{L2} = I_{C4} + I_{C6}$

$\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$

$\Delta I = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5})$

$$\Delta I = I_{EE}\left[\tanh\left(\frac{V_1}{2V_T}\right)\tanh\left(\frac{V_2}{2V_T}\right)\right]$$

$$I_{C3} - I_{C6} = \frac{I_{EE}}{\left(1+e^{-V_1/V_T}\right)\left(1+e^{-V_2/V_T}\right)} - \frac{I_{EE}}{\left(1+e^{V_2/V_T}\right)\left(1+e^{-V_1/V_T}\right)}$$

$$= \frac{I_{EE}}{1+e^{-V_1/V_T}}\left[\frac{1}{1+e^{-V_2/V_T}} - \frac{1}{1+e^{V_2/V_T}}\right]$$

$$I_3 - I_6 = \frac{I_{EE}}{1+e^{-V_1/V_T}} \tanh \frac{V_2}{2V_T}$$

$$I_{C4} - I_{C5} = \frac{I_{EE}}{(1+e^{V_1/V_T})(1+e^{-V_2/V_T})} - \frac{I_{EE}}{(1+e^{V_1/V_T})(1+e^{V_2/V_T})}$$

$$= \frac{I_{EE}}{1+e^{V_1/V_T}} \left[\frac{1}{1+e^{-V_2/V_T}} - \frac{1}{1+e^{V_2/V_T}} \right]$$

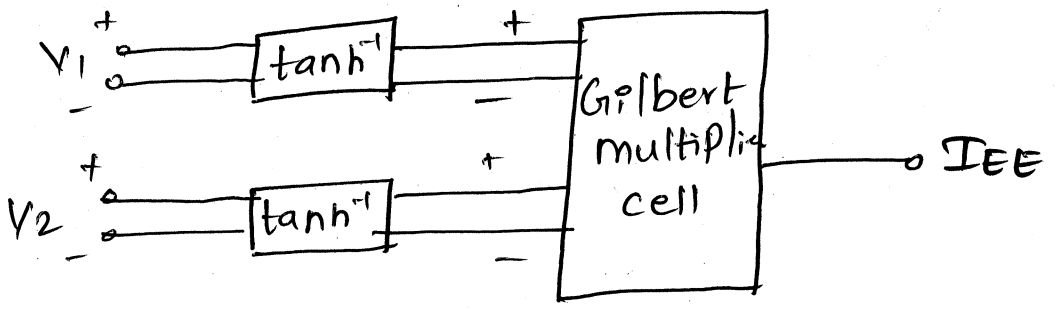
$$I_{C4} - I_{C5} = \frac{I_{EE}}{1+e^{V_1/V_T}} \tanh \frac{V_2}{2V_T}$$

$$\Delta I = \frac{I_{EE}}{1+e^{-V_1/V_T}} \tanh \frac{V_2}{2V_T} - \frac{I_{EE}}{1+e^{V_1/V_T}} \tanh \frac{V_2}{2V_T}$$

$$= I_{EE} \tanh \frac{V_2}{2V_T} \left[\frac{1}{1+e^{-V_1/V_T}} - \frac{1}{1+e^{V_1/V_T}} \right]$$

$$\Delta I = I_{EE} \tanh\left(\frac{V_2}{2V_T}\right) \tanh\left(\frac{V_1}{2V_T}\right)$$

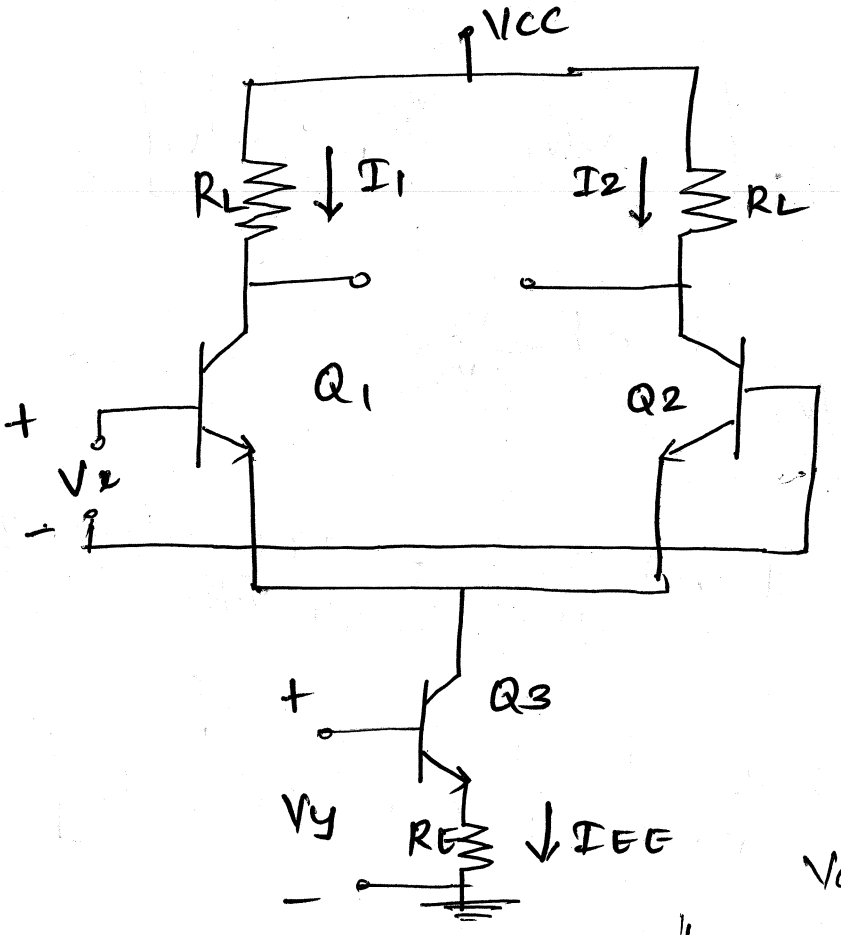
Gilbert multiplier cell with predistortion



APPLICATIONS:

* Used in modulators in communication system
* used as phase detectors
* Used as frealuency doublers, saluarer etc.

VARIABLE TRANSCONDUCTANCE TECHNIQUE MULTIPLIERS:



* A simple diff - erential circui arrangement producing the principle of Variable Trans conductance Techniaflue multiplier.

The relationship between Vo and Vx

$V_o = g_m R_L V_x$

$g_m = \frac{I_{EE}}{V_T}$

Transconductance of stage

*Vy is input to the reference current source of the differential amplifier.

$V_o = \frac{I_{EE} \cdot R_L \cdot V_x}{V_T}$

$= \frac{V_y}{V_T R_E} R_L V_x$

$V_o = V_x . V_y . \frac{R_L}{V_T R_E}$

Note: $I = \frac{V}{R}$

$I_{EE} = \frac{V_y}{R_E}$

Consider $\frac{R_L}{V_T R_E} = K$

$V_o = K V_x V_y$

K → scaling Factor

EXPLAIN THE BASIC BLOCK DIAGRAM OF ADC and DAC?

* MOST of the real world physical quantities such as voltage, current, temperature, pressure are available in analog form.
* Even though an analog signal represents a real physical parameter with accuracy.
* For processing, transmission and storage purposes, it is often convenient to express these variables in digital form.
* It gives better accuracy and reduces noise.
* The operation of any digital communication is based upon analog to digital and digital to analog conversion.

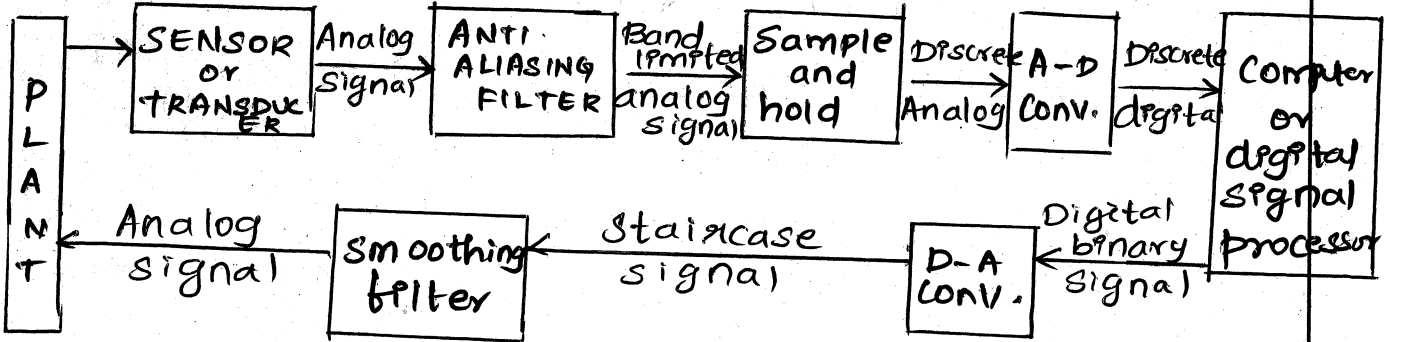


FIG: CIRCUIT SHOWING APPLICATION OF A/D and D/A CONVERTER

* The analog signal obtained from the transducer is bandlimited by antialiasing filter.
* The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.

* The sampled signal has to be held constant while conversion taking place in A/D converter.
* This requires that ADC should be preceded by a sample and hold circuit.
* The ADC output is a sequence in binary digit.
* The micro computer or digital signal processor performs the numerical calculations of the desired control algorithm.
* The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC.
* The D/A converter is usually operated at the same frequency as the ADC.
* The output of D/A converter is commonly a staircase.
* This staircase-like digital output is passed through the smoothing filter to reduce the effect of quantization noise.
* Both ADC and DAC are also known as data converters and are available in IC Form.
* It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error.

APPLICATIONS:

* Digital audio recording
* pulse code modulation transmission
* Data acaluistion
* Digital multimeter
* Digital signal processing
* Microprocessor based Instrumentation.

EXPLAIN IN DETAIL ABOUT DAC TECHNIQUES AND ITS TYPES OF DAC?

DACE
Cultivating Technology

* The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal.

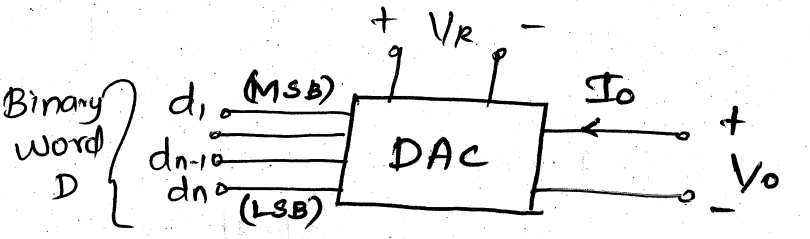


FIG: SCHEMATIC OF DAC

* The output of DAC can be either a voltage or current

* For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K V_{FS} \left(d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{n} \right)$$

V_o = Output Voltage

K = Scaling factor usually adjusted to unity.

V_{FS} = Full Scale output Voltage.

$d_1, d_2, .. d_n$ = n-bit binary word

d_1 = most significant bit with a weight of $V_{FS}/2$

d_n = Least significant bit with a weight of $V_{FS}/2^n$

TYPES OF DAC:

1. Weighted Resistor DAC
2. R-2R Ladder
3. Inverted R-2R Ladder

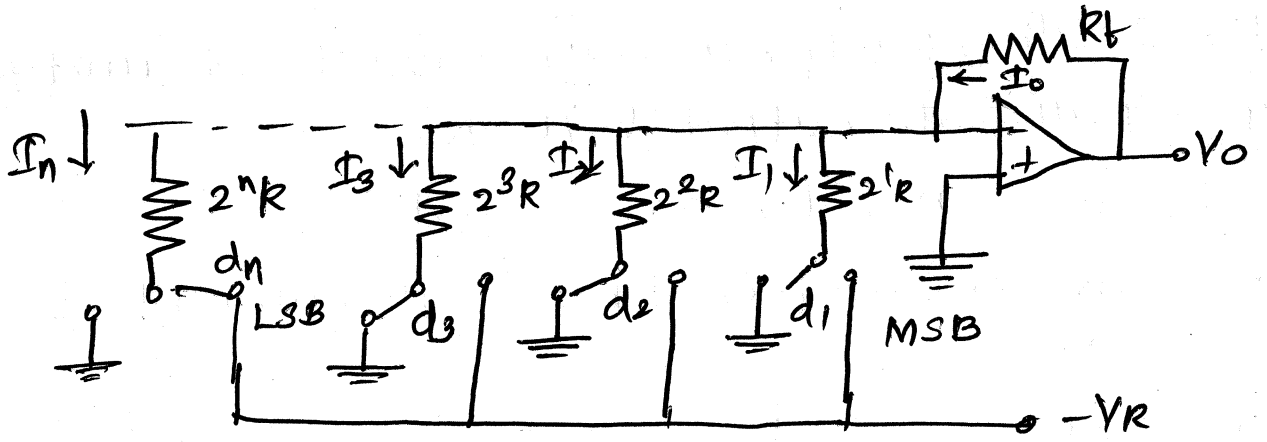
WEIGHTED RESISTOR DAC:

* It uses a summing amplifier with a binary weighted resistor network.
* It has n-electronic switches $d_1, d_2, \ldots d_n$ controlled by binary input word
* These switches are single pole double throw (SPDT) type.
* If the binary input to a particular switch is 1 it connects to the resistance of the reference voltage ($-V_R$).
* If the input is 0, the switch connects resistor to the ground.

* The output current I_o for an Ideal op-amp can be written as

$$I_o = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d^1 + \frac{V_R}{2^2 R} d^2 + \frac{V_R}{2^3 R} d^3 + \ldots + \frac{V_R}{2^n R} d_n$$



A SIMPLE WEIGHTED RESISTOR DAC

$$= \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}\right)$$

The output Voltage

$$V_o = I_o R_f$$

$$= V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}\right) \quad \text{— (1)}$$

Basic DAC evaluation:

$$V_o = K V_{FS}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}\right) \quad \text{---} (2)$$

Comparing evaluation (1) and (2)

$R_f = R$ and then $K = 1$ and $V_{FS} = V_R$

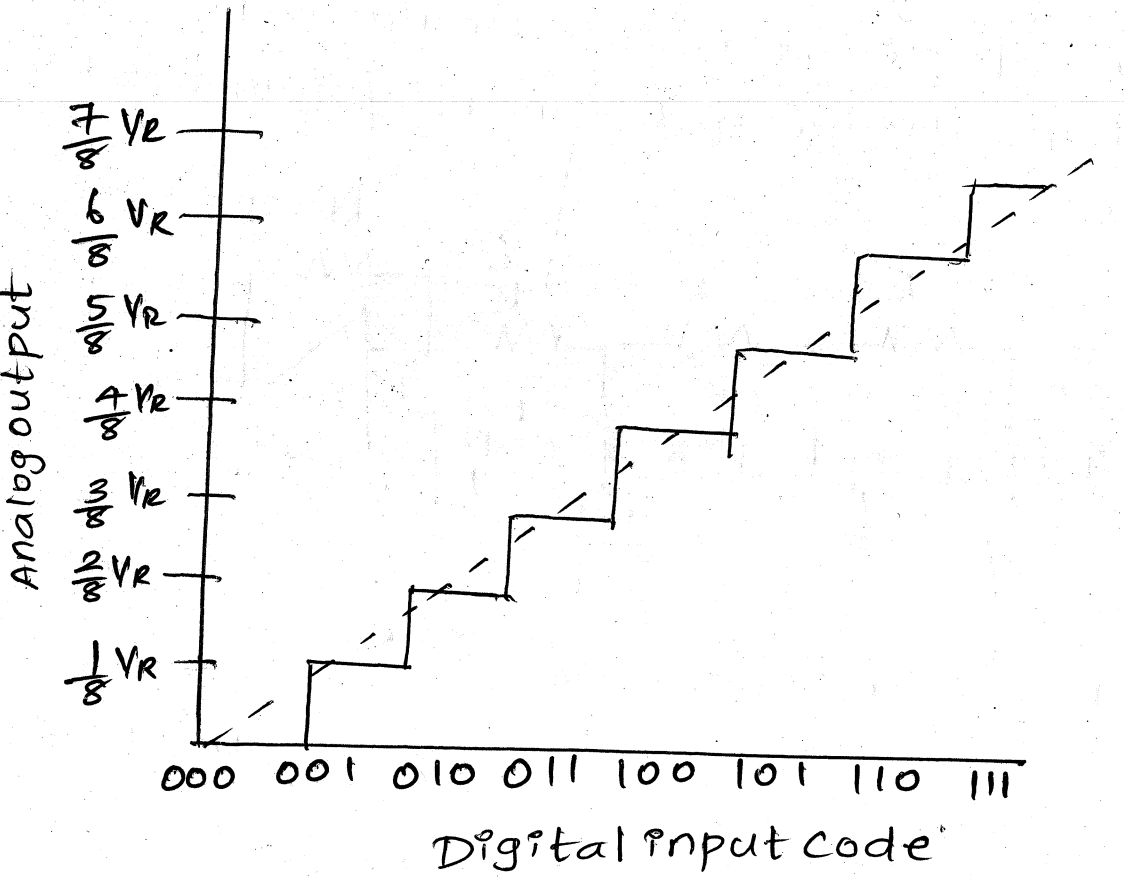


FIG: TRANSFER CHARACTERISTICS OF A 3-BIT DAC

* The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature.
* one of the disadvantages of binary weighted type DAC is the wide range of resistor values required.

* It may be observed that for better resolution, the binary word length has to be increased.
* The switches are in series with resistors and therefore, their on resistance must be very low and they should have zero offset voltage

R-2R LADDER DAC:

* Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R Ladder type DAC where only two values of resistors are required.
* The typical value of R ranges from 2.5 KΩ to 10 KΩ.

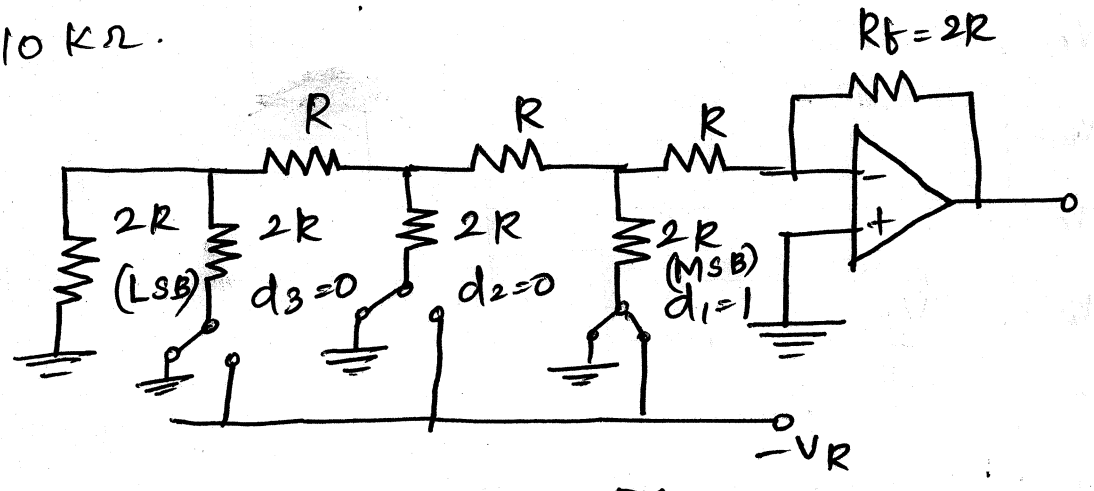


FIG: R-2R LADDER DAC

* Here the R-2R Ladder DAC is having 100 bit.

o/p of 001 bit DAC →

$$V_o = \left(\frac{-2R}{R}\right)\left(\frac{-V_R}{16}\right)$$

$$V_o = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R + \frac{2}{3}R} = \frac{-V_R}{4}$$

$$V_o = \frac{-2R}{R}\left(\frac{-V_R}{4}\right)$$

$$= \frac{V_R}{2} = \frac{V_{FS}}{2}$$

↗ output of 100-3bit DAC

INVERTED R-2R LADDER:

* In weighted Resistor type and R-2R ladder type DAC → current flowing in the resistor changes as the input data changes
* More power dissipation causes heating, which in turn creates non-linearity in DAC
* This problem can be avoided by inverted R-2R ladder DAC.
* Position of MSB and LSB interchanged
* Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground.
* since both the terminals of switches d, is at logical '0'. → The current flows through left on to the ground.
* logical '1' → to the right, the current through 2R sinks to the virtual ground.
* The circuit has the important property that the current divides equally at each of the nodes

$$I_1 = \frac{V_R}{2R} \; ; \; I_2 = \frac{V_R/2}{2R} = \frac{I_1}{2^{n-1}}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{I_1}{4} \; ; \; \text{general} \; ; \; I_n = \frac{I_1}{2^{n-1}}$$

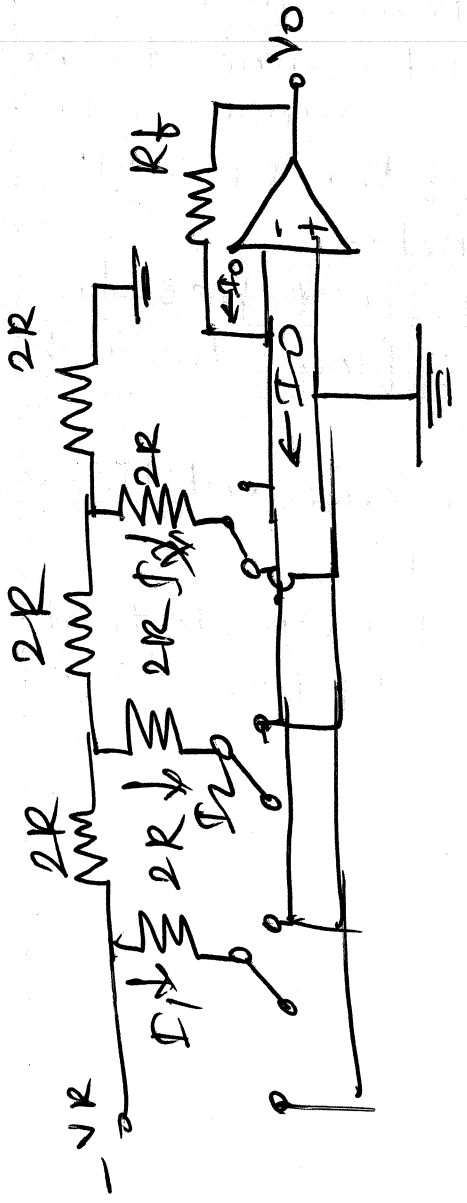
$$V_o = I_o R = -R\left[I_1 + I_2 + I_3\right]$$

$$V_o = -R\left[I_1 + \frac{I_1}{2} + \frac{I_1}{4}\right]$$

$$= -R\left[\frac{V_R}{2R}d_1 + \frac{V_R}{4R}d_2 + \frac{V_R}{8R}d_3\right]$$

$$= -R\frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

$$V_0 = -V_R\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

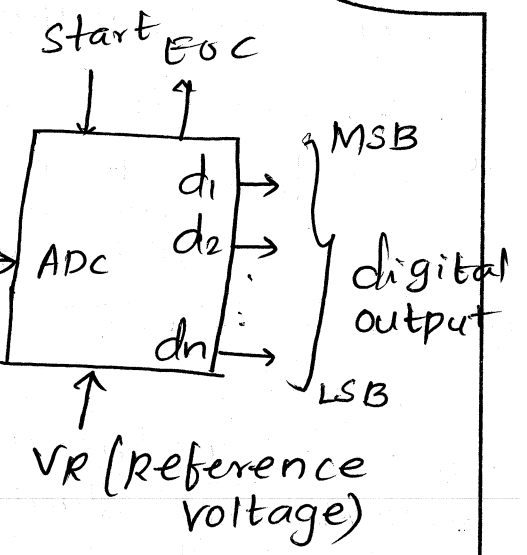


(a) INVERTED R-2R LADDER DAC

ANALOG TO DIGITAL CONVERTERS :

* The ADC is used for the purpose of converting analog to digital.

* It accepts are analog input voltage Va and produces binary $d_1, d_2, \ldots d_n$.



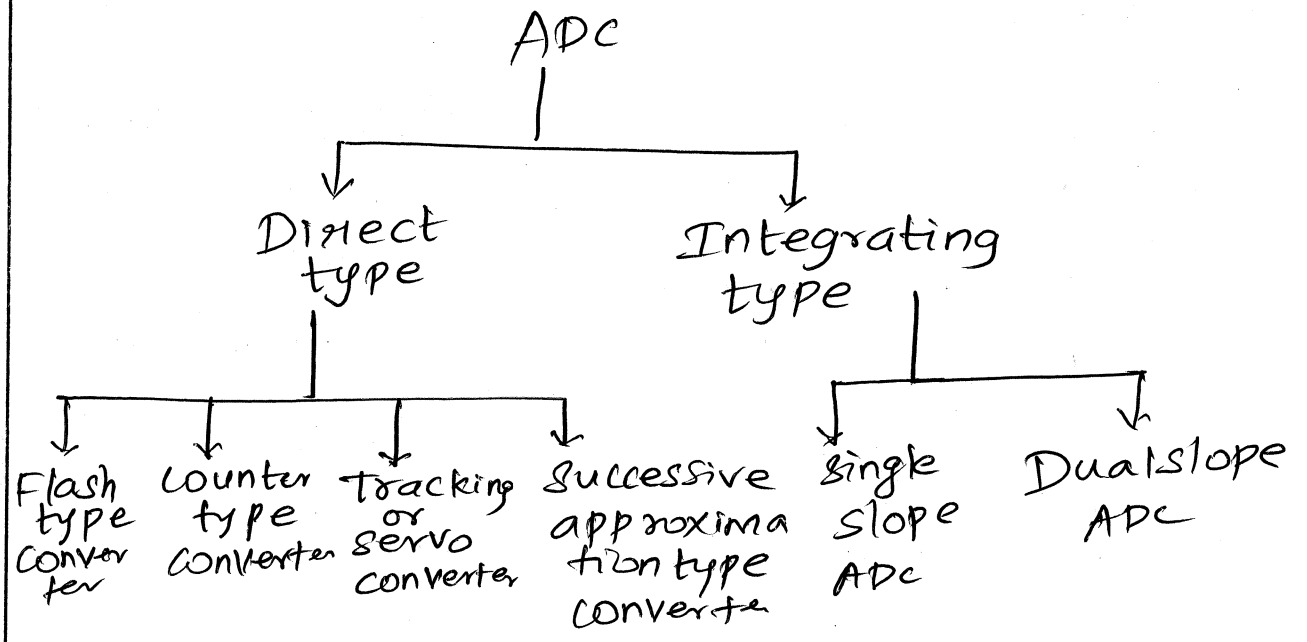
$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}$$

d_1 → Most significant bit (MSB)

d_n → Least significant bit (LSB)

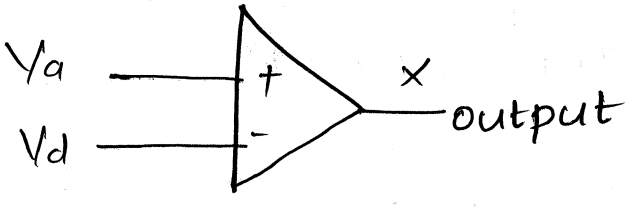
* ADC has two additional control lines START input to tell the ADC where to start conversion and EOC to announce when conversion is complete.

* Dependent on the type of application ADCs are designed for microprocessor interfacing or to directly drive LCD or Led display.



(i) PARALLEL COMPARATOR (OR) FLASH TYPE ADC CONVERTER

* This type of ADC is also called Simultaneous type or parallel comparator ADC.
  - → Simplest ADC
  - → fastest and most expensive
* The circuit consist of resistive divider network, 8 op-amp comparators and 8 to 3 line priority encoder.
* since all the resistors in resistive divider net-work are equal. So the voltage levels at the nodes are equally divided between V_R to ground.
* The comparator compares the analog input voltage Va with each of the node voltage and produce the output.
* The circuit consists of $2^n - 1$ comparators.
* The analog input signal is applied to non-inverting terminal of all comparators and the comparative voltage is derived from reference voltage using potential divider rule.



Voltage input	Logical output x
Va > Vd	x = 1
Va < Vd	x = 0
Va = Vd	previous value

* In the basic comparator, if input Va greater than potential divider voltage (or) reference voltage of that comparator (Va < Vd). The output is equal to 1. If Va is less than reference voltage (Va < Vd), the output is 0.

Truth table:

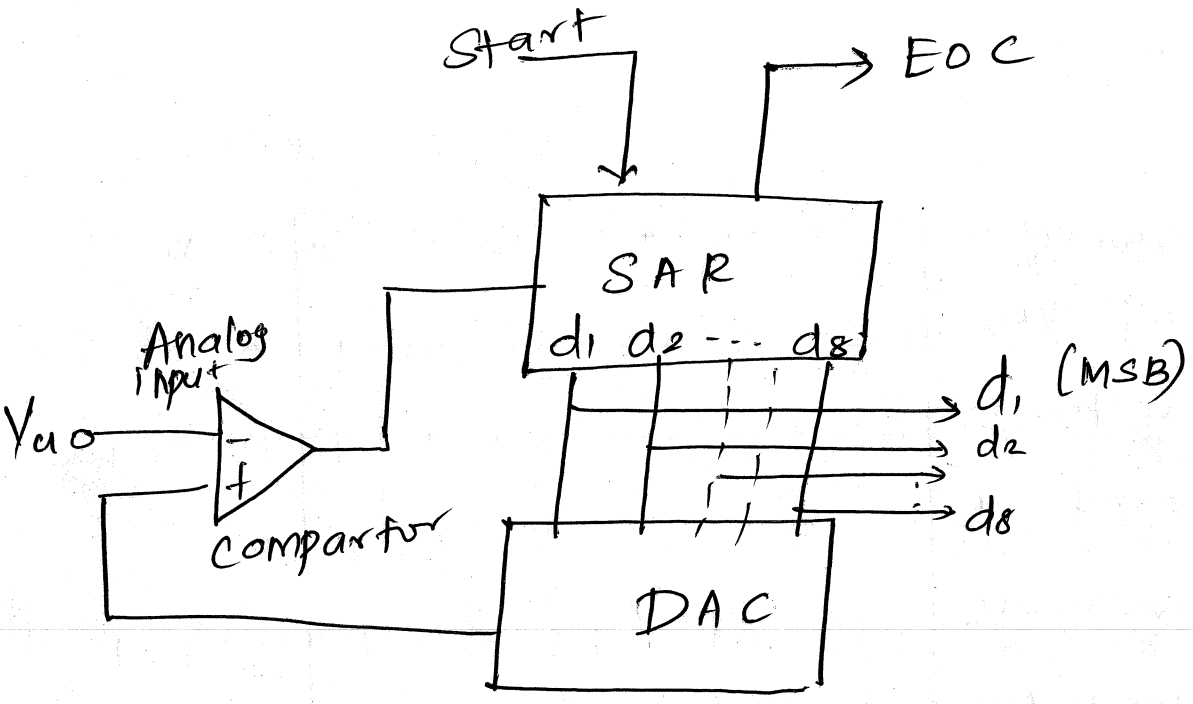
Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

TRUTHTABLE FOR 3 BIT FLASH TYPE A/D CONVERTER

DISADVANTAGE:

* $2^n - 1$ comparators need.
* The number of comparators doubles for each added bit. A 2-bit adc requires 3 comparators while for 3-bit ADC requires 7 comparators; approximately doubles for each added bit.

SUCCESSIVE APPROXIMATION TYPE A/D CONVERTER



SUCCESSIVE APPROXIMATION TYPE DAC

* The successive approximation technique complete n-bit conversion in just n-clock periods.
* An eight bit A/D converts would requires 8 clock pulses to obtain digital output
* SAR is successive approximation register to find the required value of each bit by trial and error.
* With the arrival of start command, the SAR sets the MSB, $d_1 = 1$ with all other bits to zero, so that trial code is 1000000. The output Vd of DAC is now compared with analog input Va.
* If $Va > Vd$, then 10000000 is less than the correct digital representation. The MSB is left at 1 and the next lower significant bit is made and further tested.

* If Va less than the DAC output, then 100000000 is greater than the correct digital representation. MSB to 0 and go on to the next lower significant bit.
* It required 8 clock pulses to produce the correct digital output of the analog input additional clock pulse is used to load the o/p register and reinitialize the circuit

correct digital representation	Vd at different stage of conversion	comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

* The drawback of this technique is slow speed, the number of clock pulses equal to number of conversions & clock cycles need to convert 3 bit ADC.