EEE - II ND YEAR

EE8451

LINEAR INTEGRATED CIRCUITS

AND

APPLICATIONS

UNIT - II

CHARACTERISTICS OF AMP

1. DC CHARACTERISTICS OF OPERATIONAL AMPLIFIER.

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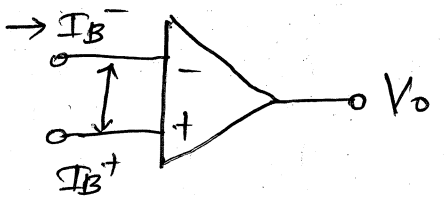
* In Ideal op-amp draws no current from the source and it is response also independent of temperature
* Both inputs are zero means output is also 0. but real op-amp have some output voltage even with both the inputs is zero.

NON IDEAL DC CHARACTERISTICS OF AN OP-AMP:

1. Input bias current
2. Input offset voltage
3. Input offset current
4. Thermal drift

INPUT BIAS CURRENT:

* In a practical op-amp base currents entering the inverting and non-inverting terminal of an op-amp.



* Even though both the transistor are Identical I_B^- & I_B^+ are not exactly equal. Due to internal imbalances.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

Consider $I_B = 500nA$

$V_i = 0$, so the output

$V_o = I_B R_F$; $R_F = 1M\Omega$

$V_o = 500 \times 10^{-9} \times 1 \times 10^6$

$\boxed{V_o = 500\ mV}$

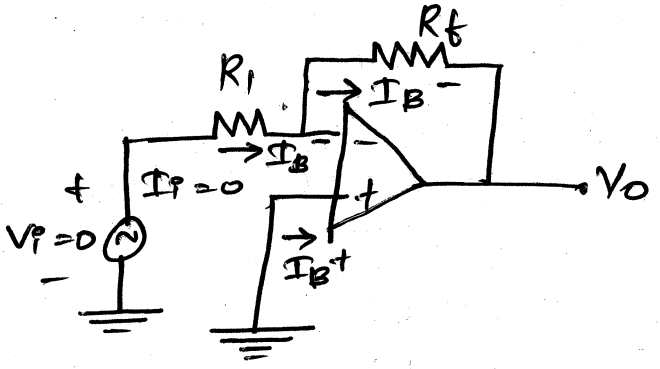


FIG: INVERTING AMPLIFIER WITH BIAS CURRENTS

In that figure, input is 0V, output will be 500 mV. So we need compensation technique to make output is zero for zero input.

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Input Bias current compensation:

* To compensate the Input Bias current compensation resistor is connected in the non-inverting terminal of an op-amp.

I_B^+ entering to Rcomp the voltage is V_1

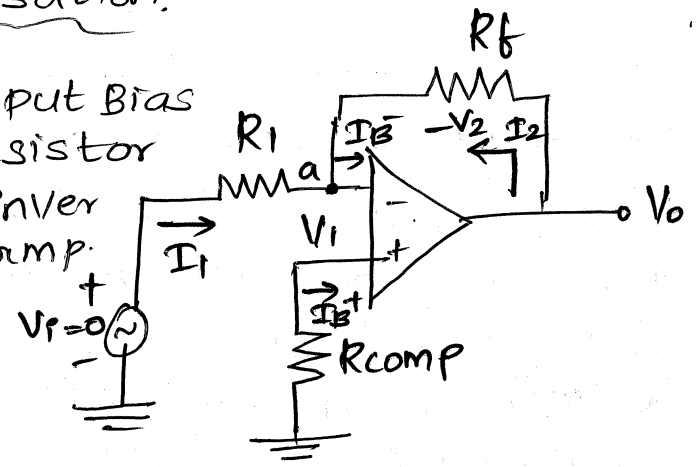


FIG. INVERTING AMPLIFIER WITH BIAS CURRENT COMPENSATION

Apply the KVL

$$-V_1 + 0 + V_2 - V_o = 0$$

$$V_o = V_2 - V_1$$

* By choosing proper value of Rcomp decide V_1 and to be cancelled V_2. Now $V_o = 0$.

$$V_1 = I_B^+ R_{comp}$$

$$I_B^+ = \frac{V_1}{R_{comp}}$$

If $V_i = 0$, $i = \frac{V_1}{R_1}$

$$I_2 = \frac{V_2}{R_f}$$

For compensation, $V_o = 0$

$V_i = 0$, sub $V_1 = V_2$

$$I_2 = \frac{V_1}{R_f}$$

KCl at node 'a', $I_B^- = I_2 + I_1$

$$I_B^- = \frac{V_1}{R_f} + \frac{V_1}{R_1}$$

$$= V_1\left[\frac{1}{R_f} + \frac{1}{R_1}\right]$$

$$I_B^- = I_B^+$$

$$I_B^+ = V_1\left[\frac{R_1 + R_f}{R_1 R_f}\right]$$

$$I_B^+ = V_1 / R_{comp}$$

$$\frac{V_1}{R_{comp}} = V_1\left[\frac{R_1 + R_f}{R_1 R_f}\right]$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$$

$$R_{comp} = R_1 \parallel R_f$$

INPUT OFFSET CURRENT:

* Input bias current compensation will work if both bias currents I_B^- and I_B^+ are ealual.
* Input transistors cannot be made identical, it has small difference between I_B^- and I_B^+, the difference is called input offset current.

$$I_{os} = I_B^+ - I_B^-$$

The input offset current typical value is 200nA

From Bias current compensation circuit

$$V_1 = I_B^- R_{comp} \quad \text{——} (1)$$

$V_1 = 0$, at node 'a' virtual terminal

$$I_1 = \frac{V_1}{R_1} \quad \text{——} (2)$$

apply the KVL at node 'a'

$$I_B^- = I_2 + I_1$$

$$I_2 = I_B^- - I_1 \quad \text{——} (3)$$

Substitute I_1 from equation (2)

$$I_2 = I_B^- - \frac{V_1}{R_1}$$

Substitute V_1 from equation (1)

$$I_2 = I_B^- - \frac{I_B^- R_{comp}}{R_1} \quad \text{——} (4)$$

We know that

$$V_o = \left(I_B^- - \frac{I_B^+ R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp} \quad \text{——} (5)$$

Substitute $R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$ in equation (5)

$$V_o = \left[I_B^- - \frac{I_B^+ R_1 R_f}{R_1 (R_1 + R_f)}\right] R_f - I_B^+ \left(\frac{R_1 R_f}{R_1 + R_f}\right)$$

$$V_o = \left[\frac{I_B^- R_1 (R_1 + R_f) - I_B^+ R_1 R_f}{R_1 (R_1 + R_f)}\right] R_f - \frac{I_B^+ R_1 R_f}{R_1 + R_f}$$

$$= \frac{I_B^- R_1 R_f (R_1 + R_f) - I_B^+ R_1 R_f^2 - I_B^+ R_1 R_f}{R_1 + R_f}$$

$$= \frac{I_B^- R_1^2 R_f + I_B^- R_1 R_f^2 - I_B^+ R_1 R_f^2 - I_B^+ R_1 R_f}{R_1 + R_f}$$

$$= \frac{I_B^- R_1^2 R_f + (I_B^- - I_B^+) R_1 R_f^2 - I_B^+ R_1 R_f}{R_1 + R_f}$$

$$= \frac{(I_B^- - I_B^+) R_1 R_f^2 + I_B^- R_1^2 R_f - I_B^+ R_1 R_f}{R_1 + R_f}$$

$$= \frac{(I_B^- - I_B^+)(R_1 R_f + R_f^2)}{(R_1 + R_f)(R_1 + R_f)} = \frac{(I_B^- - I_B^+)(R_1 + R_f) R_f}{(R_1 + R_f)}$$

$$V_o = (I_B^- - I_B^+) R_f$$

$$\boxed{V_o = |I_{OS}| R_f}$$

R_f is replaced as T feedback network compensate the input offset current

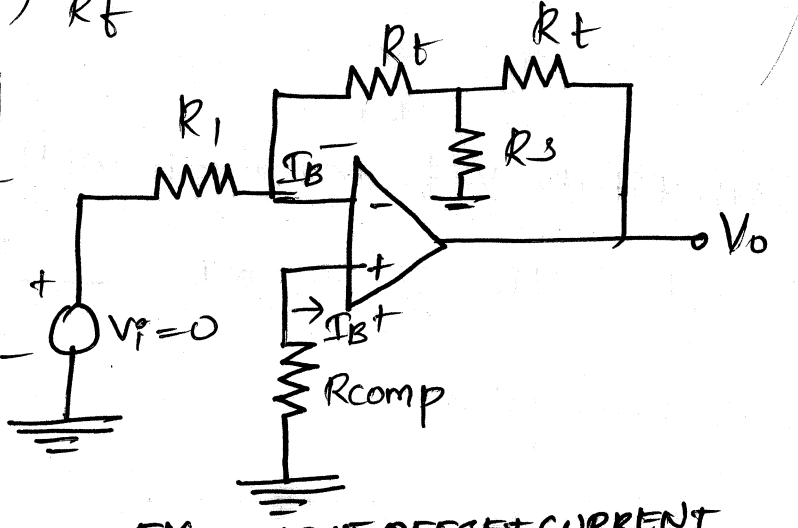
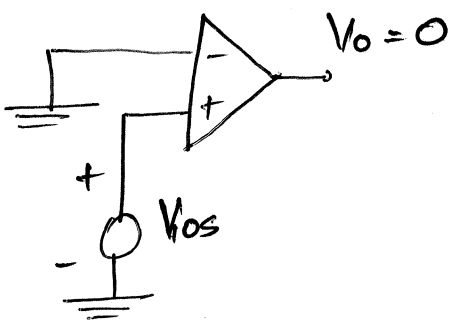


FIG. INPUT OFFSET CURRENT COMPENSATION

INPUT OFFSET VOLTAGE:

* still there is some output voltage for 0 input voltage due to unavoidable imbalance.
* TO apply small voltage at input terminals to make output voltage is 0 that is called input offset voltage.



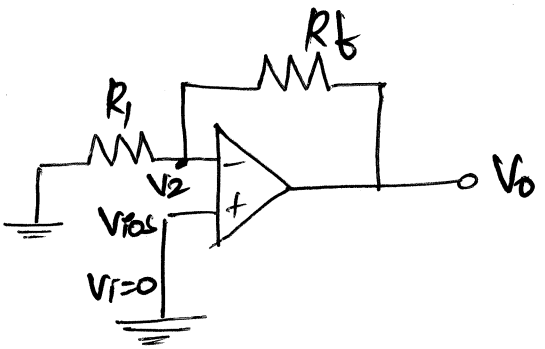


FIG. NON INVERTING AMPLIFIER WITH INPUT

Use potential divider rule:

$$V_2 = V_o \frac{R_1}{R_1 + R_f}$$

$$V_o = V_2 \left(\frac{R_f + R_1}{R_1} \right)$$

$$V_o = V_2 \left(1 + \frac{R_f}{R_1} \right)$$

$$V_{ios} = |V_i - V_2|$$

$$V_i = 0$$

$$V_{ios} = |0 - V_2|$$

$$V_o = \left(1 + \frac{R_f}{R_1} \right) V_{ios}$$

To supply the input offset voltage make the output is zero.

THERMAL DRIFT:

* The parameters I_B, I_{os} and V_{ios}.
* Bias current, offset current and offset voltage changes with temperature.
* The circuit carefully nulled at 25°C may not remains so when the temperature rises to 35°C. This is called drift.
* Thermal drift causes voltage and current to change.
* The average rate of change of input offset voltage per unit change in temperature is known as thermal voltage drift.

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2. AC CHARACTERISTICS OF OP-AMP

* When an Ac input signal applied to op-amp, the following Ac characteristics are analyzed

(i) FREQUENCY RESPONSE
(ii) SLEW RATE

FREQUENCY RESPONSE:

* Ideal op-amp has infinite Bandwidth this means that for dc signal open loop gain (A_{OL}) 90dB pt is same as 90dB for audio and radio high frequencies but practical op-amp A_{OL} decreases at higher frequencies.

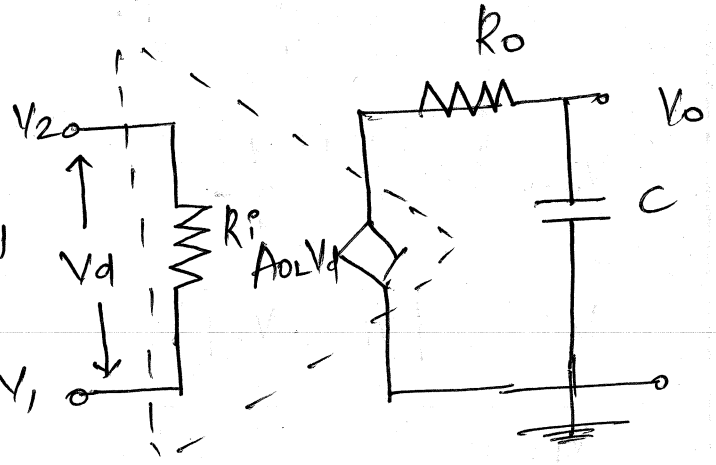

FIG. HIGH FREQUENCY EQUIVALENT CIRCUIT OF OP-AMP

* capacitance due to physical characteristics of the device.
* For op-amp only one break frequency.

$$V_o = \frac{-jX_c}{R_o + (-jX_c)} A_{OL} V_d$$

$$= \frac{-jX_c}{-jX_c} \cdot \frac{A_{OL} V_d}{1 - \frac{R_o}{jX_c}}$$

$$= \frac{A_{OL} V_d}{1 + j\frac{R_o}{X_c}}$$

$$X_c = \frac{1}{2\pi f C}$$

$$= \frac{A_{OL} V_d}{1 + j\frac{R_o}{\frac{1}{2\pi f C}}}$$

$$V_o = \frac{A_{OL} V_d}{1 + j(f/f_1)} \qquad f_1 = \frac{1}{2\pi R_o C}$$

$$\frac{V_o}{V_d} = \frac{A_{OL}}{1 + j(f/f_1)}$$

$$A = \frac{A_{OL}}{1 + j(f/f_1)}$$

The magnitude and phase angle

$$|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}, \quad \phi = \tan^{-1}(f/f$$

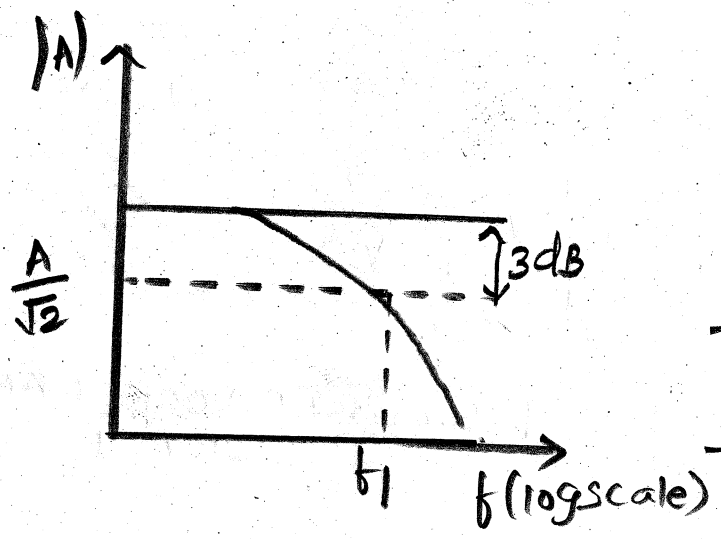

FIG. MAGNITUDE CHARACTERISTICS

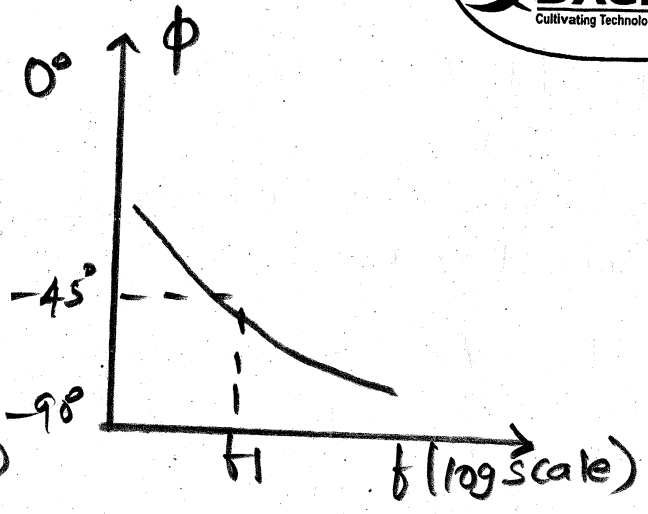

FIG. PHASE CHARACTERISTICS

MAGNITUDE CHARACTERISTICS:

1. The applied frealuency f is $f << f_1$, the gain maximum, |A|
2. at $f = f_1$, the gain is 3dB down the maximum gain, $\frac{A}{\sqrt{2}} = 0.707|A|$
3. when the input frealuency $f >> f_1$ the gain start roll of at a rate of -20dB/decade. Increase in Frealuency.

PHASE CHARACTERISTICS:

1. When the applied frealuency $f << f_1$, phase shift ϕ is 0°
2. at $f = f_1$, the phase shift is $\phi = -45$
3. When $f >> f_1$, the phase shift is $\phi = -90°$

Stability of an op-amp:

Closed loop Transfer function,

$$A_{CL} = \frac{A}{1 + AB} \quad \text{---} \quad (1)$$

A → openloopgain

β → Feedback Ratio

If $(1+A\beta) = 0$

↓

circuit will become unstable.

$1-(-A\beta) = 0$

$-A\beta = 1$

$|A\beta| = 1$

$\angle -A\beta = 0 \rightarrow$ multiple of 2π

$\angle -A\beta = \pi \rightarrow$ odd multiple of π

The instability means

$(1+A\beta) < 1$

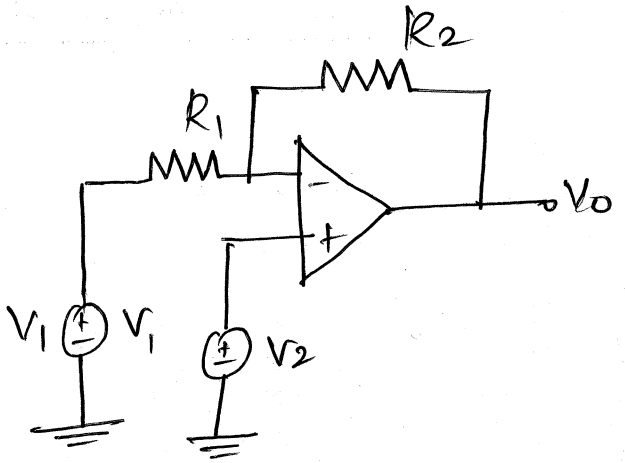

FIG. CLOSED LOOP OF AN OP-AMP

FREQUENCY COMPENSATION TECHNIQUES

* We need op-amp applications, large bandwidth and lower closed loop gain by applying suitable frealuency compensation method.

→ Dominant pole compensation

→ pole zero compensation

(i) DOMINANT POLE COMPENSATION

* A → Un compensation Transfer functions of an operational amplifier.

* Introduce a dominant pole by adding RC network in series with the OP-amp.

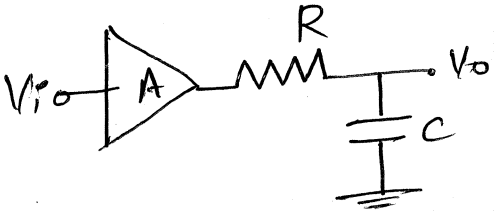

FIG. DOMINANT POLE COMPENSATION

The compensated Transfer function,

$$A' = \frac{V_o}{V_i}$$

$$A' = A \frac{-j/\omega C}{R - j/\omega C}$$

$$A' = \frac{-j/\omega C}{-j/\omega C} \frac{A}{1 - R/j\omega C}$$

$$A' = \frac{A}{1 + RJ\omega C} \quad \therefore \omega = 2\pi f c$$

$$A' = \frac{A}{1 + j2\pi fRC}$$

$$A' = \frac{A}{1 + j(f/fd)} \quad \therefore fd = \frac{1}{2\pi RC}$$

$$A' = \frac{A_{OL}}{(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)} \times \frac{1}{1 + j.(f/fd)}$$

$$fd < f_1 < f_2 < f_3$$

* The Value of fd choose by R and C introducing the pole, the slope crossing the corner frealuency f_1.

* uncompensated transfer function. A providing negligible phase shift

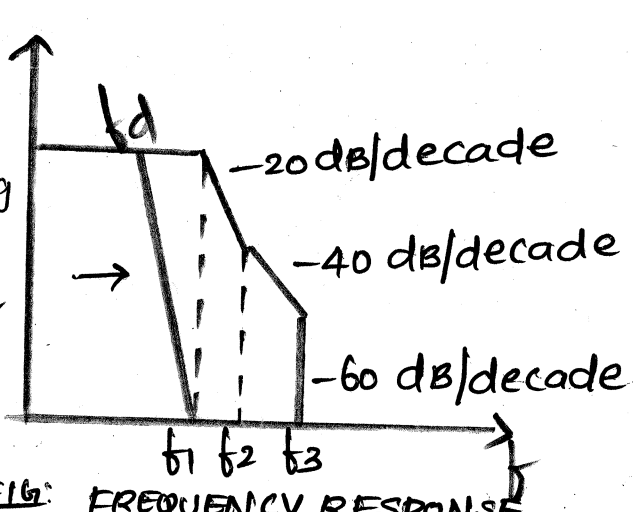

FIG: FREQUENCY RESPONSE

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(ii) POLE ZERO COMPENSATION:

* In dominant pole compensation, introduce the new pole fd, reducing the bandwidth. So one more additional component R_2 series with C_2.

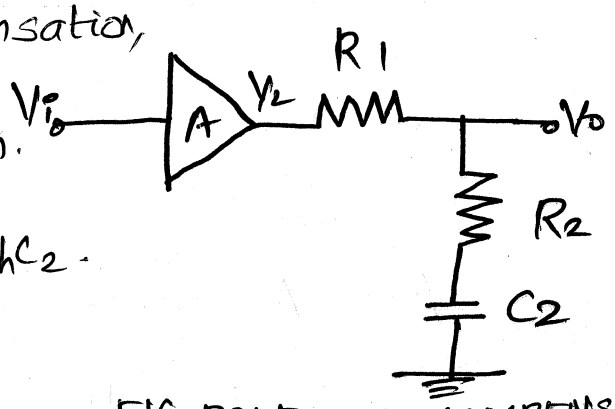

FIG POLE ZERO COMPENSATION

$$Z_1 = R_1$$

$$Z_2 = R_2 + \frac{1}{j\omega C_2}$$

$$V_o = V_2 \cdot \frac{Z_2}{Z_1 + Z_2}$$

$$V_o = V_2 \cdot \frac{R_2 + \frac{1}{j\omega C_2}}{R_1 + R_2 + \frac{1}{j\omega C_2}}$$

$$\frac{V_o}{V_2} = \frac{\frac{1 + j\omega C_2 R_2}{j\omega C_2}}{\frac{R_1 j\omega C_2 + j\omega C_2 R_2 + 1}{j\omega C_2}} = \frac{1 + j\omega C_2 R_2}{1 + j\omega C_2 R_1 + j\omega C_2 R_2}$$

$$\frac{V_o}{V_2} = \frac{1 + j\,2\pi f C_2 R_2}{1 + j\omega (R_1 + R_2) C_2} = \frac{1 + j\,2\pi f C_2 R_2}{1 + j\,2\pi f (R_1 + R_2) C_2}$$

where $f_1 = \frac{1}{2\pi R_2 C_2}$

$f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$

$$\frac{V_o}{V_2} = \frac{1 + j\,(f/f_1)}{1 + j\,(f/f_0)}$$

The overall transfer function is

$$A' = \frac{V_o}{V_i} = \frac{V_o}{V_2} \cdot \frac{V_2}{V_i}$$

$$= \frac{1 + j\,(f/f_1)}{\cdot} \cdot \frac{A_{OL}}{1 + j(f/f_1)(1 + j\,f/f_2)(1 + j\,(f/f_3)}$$

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SLEW RATE:

* For ideal OP-amp response time should be zero.
* In practical op-amp small signal output has no problem.
* For large signal output, op-amp speed limited by slew Rate.

SLEW RATE IS DEFINED AS THE MAXIMUM RATE OF CHANGE OF OUTPUT VOLTAGE CAUSED BY STEP INPUT VOLTAGE AND USUALLY SPECIFIED IN V/μs.

Causes of slew rate:

* The capacitor within or outside, which prevents the output voltage from responding immediately to fast changing input.

The rate at which voltage across the capacitor.

$$\frac{dvc}{dt} = \frac{I}{C}$$

Slew Rate of IC 741.

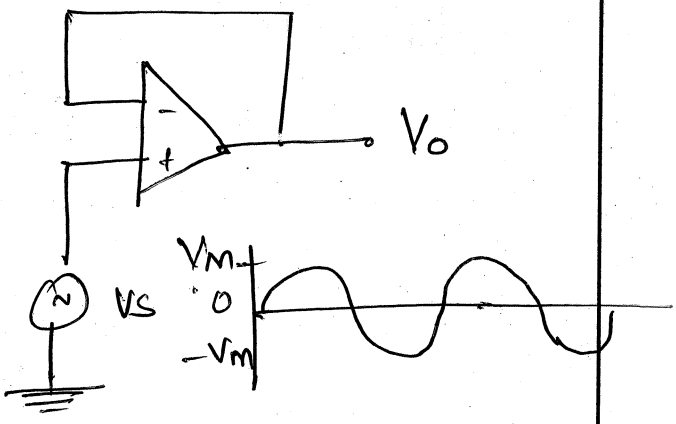
$$S.R = \frac{dvc}{dt} = \frac{I_{max}}{C}$$

$I_{max} = 15mA$

$C = 30pF$

$$= \frac{15 \times 10^{-3}}{30 \times 10^{-12}}$$

$= 0.5 V/\mu s.$



VOLTAGE FOLLOWER

* slew rate limits the response speed of all large signal wave shapes.
* Higher slew rate should have either higher current or smaller compensating capacitor.

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$V_s = V_m \sin \omega t$ —— (1)

$V_o = V_m \sin \omega t$ —— (2)

Differentiate the equation (2)

$$\frac{dV_o}{dt} = V_m \omega . \cos \omega t$$

$\cos \omega t = 1$

$$\frac{dV_o}{dt} = V_m \omega$$

$S.R = 2\pi f V_m$

$$SR = \frac{2\pi f V_m}{106} \ V/\mu s$$

f = input frequency

V_m = peak output amplitude

$$f_{max}(Hz) = \frac{\text{Slew Rate}}{6.28 \times V_m} \times 10^6$$

3. OPERATIONAL AMPLIFIER USING BJT.

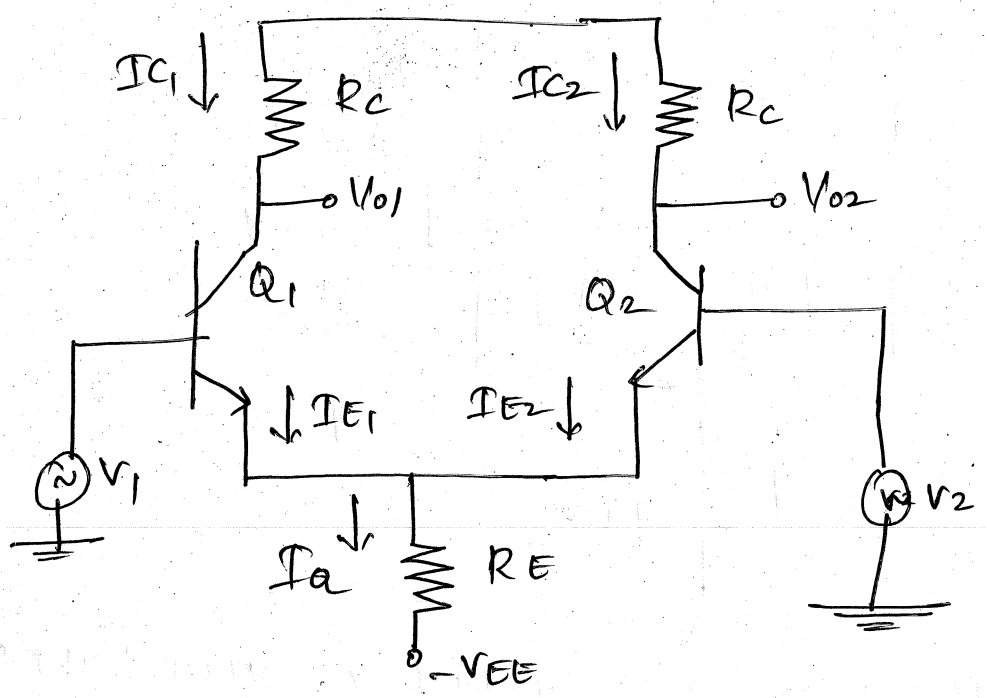


FIG: BJT DIFFERENTIAL AMPLIFIER

* This is Basic emitter coupled differential amplifier it gives high input resistance and low drift on operating point.

* B_1 → Non-inverting input terminal
* B_2 → Inverting terminal it provides a output 180° phase shift of input at the collector terminal of Q_2.

Types of operation:

(i) Common mode operation
(ii) Differential mode operation

COMMON MODE OPERATION:

* Both the bases of transistor Q_1 and Q_2 are joined together and connected to a common voltage input V_{CM}.
* Q_1 and Q_2 → Forward biased and matched due to the common voltage V_{CM}

The current I_Q divides equally $I_{E1} = \frac{I_Q}{2} = I_{E2}$.

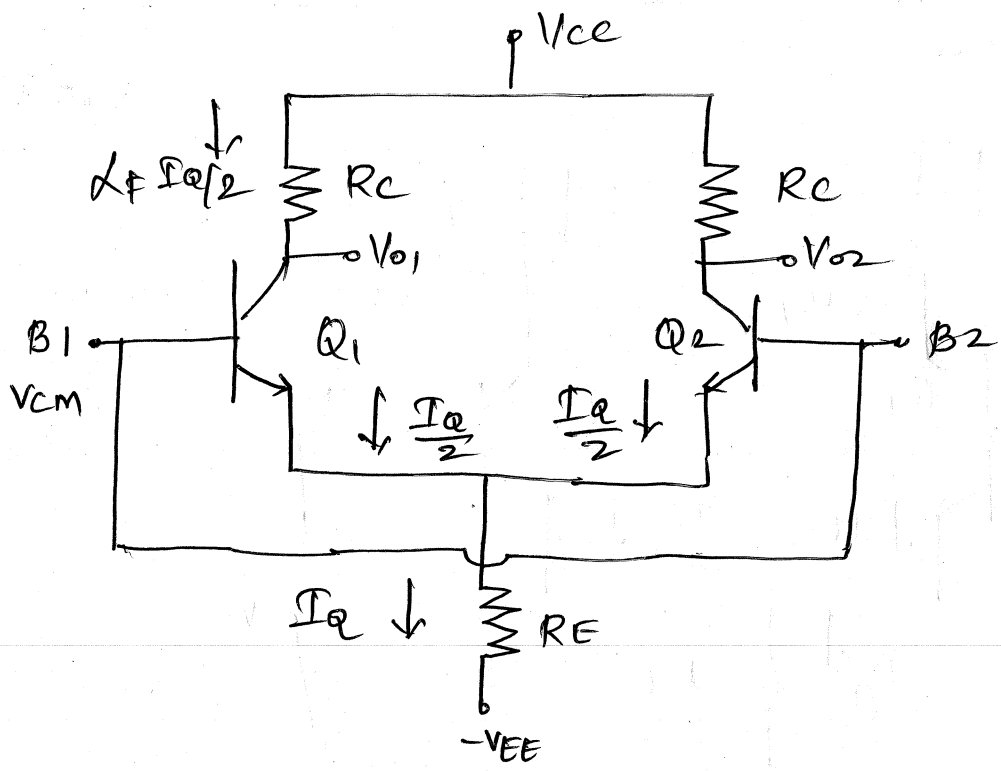


FIG. COMMON MODE OPERATION OF DIFFERENTIAL AMPLIFIER

The collector current $I_{C1} = \frac{\alpha_F I_Q}{2} = I_{C2}$

The Voltage across the collector of two transistor Q_1 and Q_2 are

Note: $V_C = V_{CC} - I_C R_C$

$$V_C = V_{CC} - \frac{\alpha_F I_Q R_C}{2}$$

Both the collector voltages are equal

$$V_{o1} = V_{CC} - \frac{\alpha_F I_Q R_C}{2}$$

$$V_{o2} = V_{CC} - \frac{\alpha_F I_Q R_C}{2}$$

$$V_{CM} = V_{o1} - V_{o2} = 0$$

* During the common mode signal output is zero.

(ii) DIFFERENTIAL MODE OPERATION:

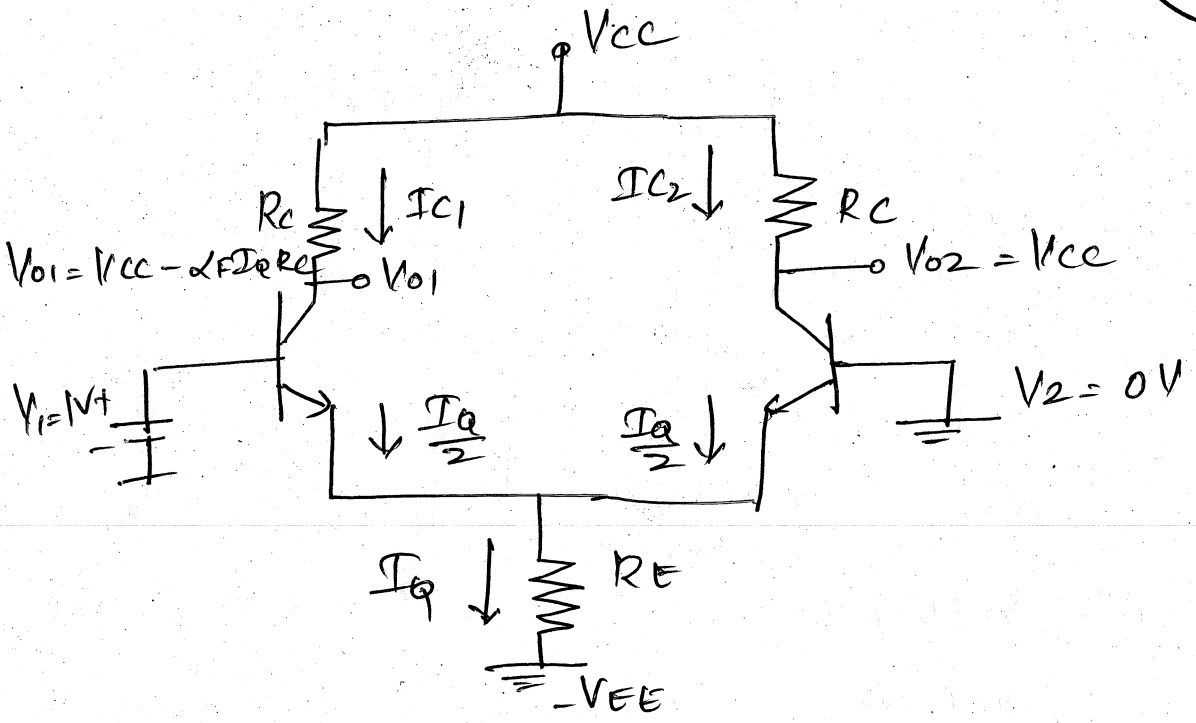


FIG: DIFFERENTIAL MODE OPERATION

CASE 1:

* 1V applied to B_1 } $Q_1 \rightarrow$ ON
* 0V applied to B_2 } $Q_2 \rightarrow$ OFF

$Q_1 \rightarrow$ Forward Biased

$Q_2 \rightarrow$ Reverse Biased

$$V_{o1} = V_{cc} - \alpha_F I_Q R_c$$

$$V_{o2} = V_{cc}$$

CASE 2:

* −1V applied to B_1 } $Q_1 \rightarrow$ OFF
* 0V applied to B_2 } $Q_2 \rightarrow$ ON

$Q_1 \rightarrow$ REVERSE BIASED

$Q_2 \rightarrow$ FORWARD BIASED

$$V_{o1} = V_{cc}$$

$$V_{o2} = V_{cc} - \alpha_F I_Q R_c$$

TRANSFER CHARACTERISTICS:

$$I_{C_1} = \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad \text{——— (1)}$$

$$I_{C_2} = \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad \text{——— (2)}$$

I_{ES} → Reverse saturation current

V_T → Thermal voltage

Divide eqn (1) ÷ (2)

$$\frac{I_{C_1}}{I_{C_2}} = \frac{\alpha_F I_{ES} e^{V_{BE1}/V_T}}{\alpha_F I_{ES} e^{V_{BE2}/V_T}}$$

$$\frac{I_{C_1}}{I_{C_2}} = \frac{e^{V_{BE1}/V_T}}{e^{V_{BE2}/V_T}}$$

$$\frac{I_{C_1}}{I_{C_2}} = e^{(V_{BE_1} - V_{BE2})/V_T} \quad \text{——— (3)}$$

Write the KVL at B-E LOOP

$$V_1 - V_{BE1} + V_{BE2} - V_2 = 0$$

$$V_1 - V_2 = V_{BE1} - V_{BE2} \quad \text{——— (4)}$$

$$V_{BE1} - V_{BE2} = V_1 - V_2 = V_d$$

$$I_Q = I_{E1} + I_{E2} = \frac{I_{C_1}}{\alpha_F} + \frac{I_{C_2}}{\alpha_F}$$

$$I_Q = \frac{I_{C_1}}{\alpha_F}\left(1 + \frac{I_{C_2}}{I_{C_1}}\right) \quad \text{——— (5)}$$

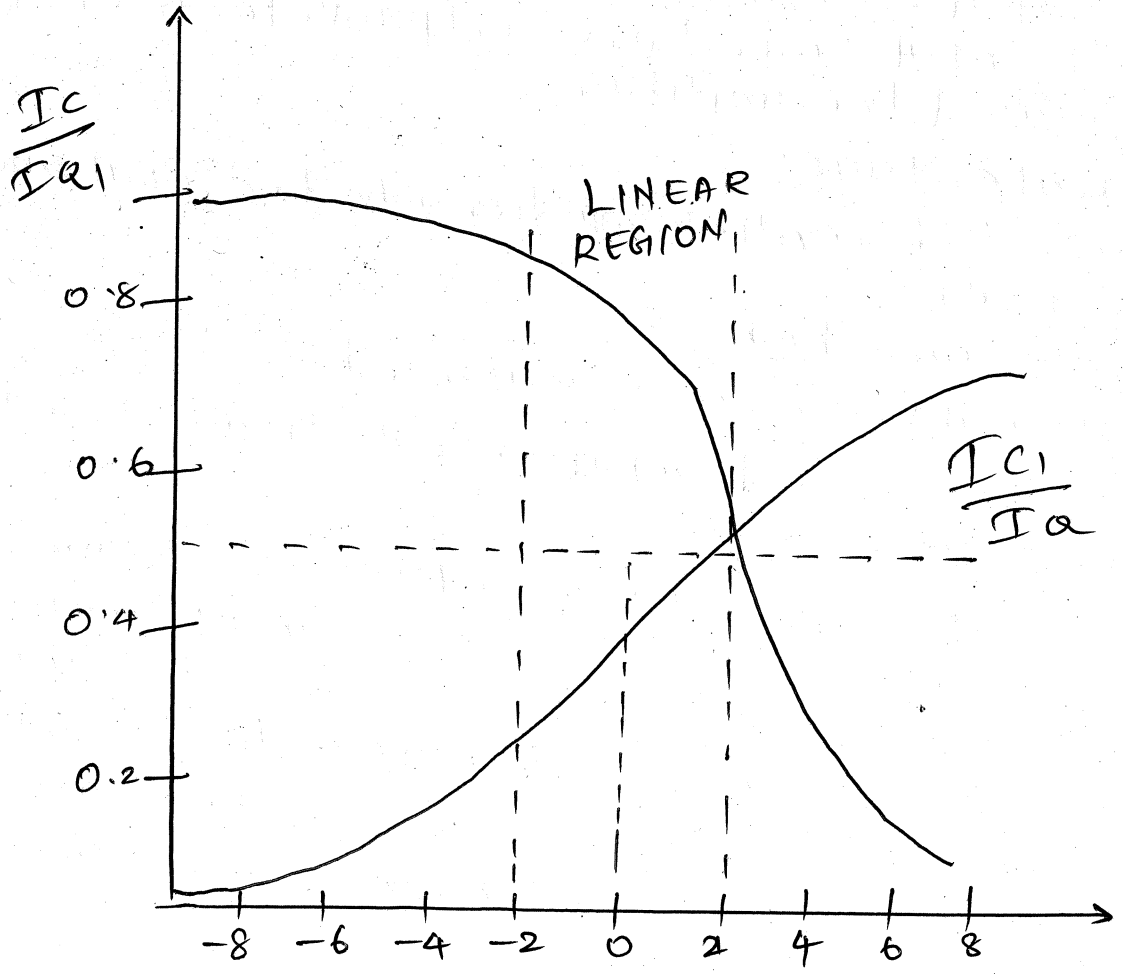
Using eqations (3) and (5)

$$\frac{I_{C_1}}{I_{C_2}} = e^{V_d/V_T} \; ; \; \frac{I_{C_2}}{I_{C_1}} = \frac{1}{e^{V_d/V_T}}$$

$$I_Q = \frac{I_{C1}}{\alpha_F}\left(1 + \frac{1}{e^{V_d/V_T}}\right)$$

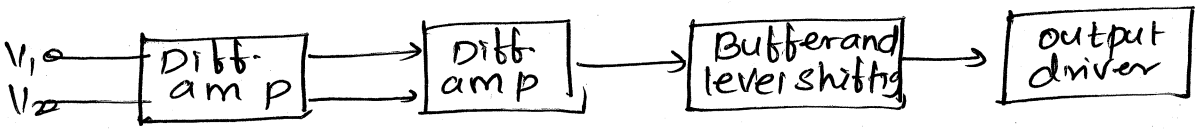
$$I_Q = \frac{I_{C1}}{\alpha_F}\left(1 + e^{-V_d/V_T}\right)$$

$$I_{C1} = \frac{\alpha_F I_Q}{1 + e^{-V_d/V_T}} \quad ; \quad I_{C2} = \frac{\alpha_F I_Q}{1 + e^{V_d/V_T}}$$



TRANSFER CHARACTERISTICS

4. OPERATIONAL AMPLIFIER STAGES:



Input stage:

* high input impedance to prevent loading on the high gain stage.
* It requires two input terminals
* low output impedance
* achieved by dual input, balanced output differential amplifier
* Diff. amplifier is to amplify the difference between the two input signals.
* high input impedance and provides most of the voltage gain of the amplifier

INtermediate stage:

* Another differential amplifier with dual input and unbalanced output.
* overall gain is high
* Additional voltage gain required
* chain of cascaded amplifiers called multistage amplifio

Level shifting stage:

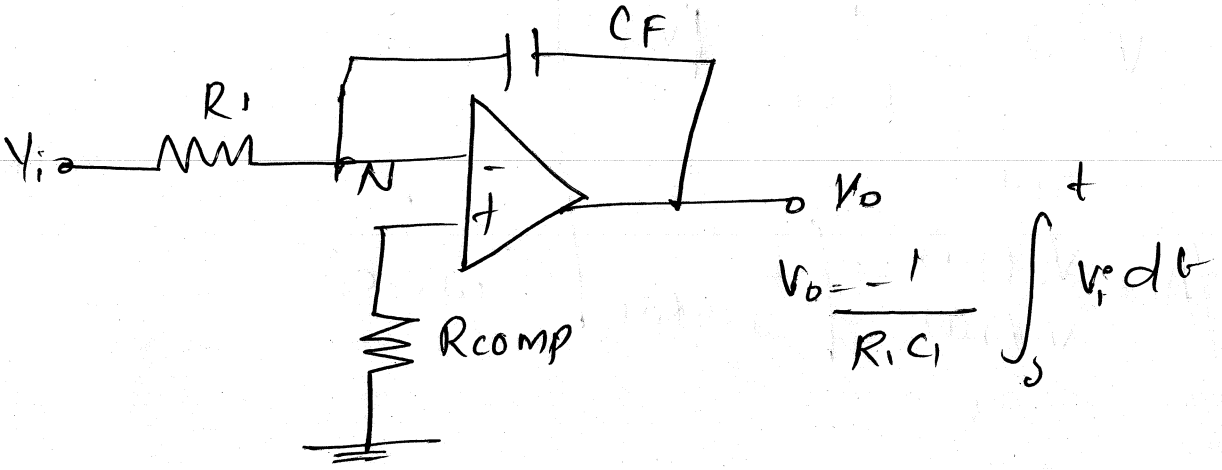
* coupling capacitors are not used to cascade the stages
* dc level increases well above ground potential.
* dc level may drive the transistors into saturation
* This cause distortion in the output due to clipping
* level shifter → d.c level down to ground potential.
* buffer → an emitter follower whose input impedance is very high.

Output stage:

* provide low input impedance, large a.c output voltage swing and high current sourcing and sinking capability.
* push-pull complementary amplifier meets all these requirements. Increases the output voltage swing
* It raises the current supplying capability of op-an

INTEGRATOR:

* To interchange the resistor and capacitor of the differentiator we have the circuit is called integrator.
* The circuit performs the mathematical operation of integrator and also used as low pass filter



ANALYSIS Nodal equation at node 'N'

$$\frac{V_i}{R_1} + C_F \frac{dv_o}{dt} = 0$$

$$\frac{dv_o}{dt} = -\frac{1}{R_F C_F} V_i$$

Integrating on both sides we get

$$\int_0^t dv_o = -\frac{1}{R_F C_F} \int_0^t V_i \, dt$$

$$V_o(t) = -\frac{1}{R_F C_F} \int_0^t V_i(t) \, dt + V_o(0)$$

$V_o(0) = 0V$

$$V_o(t) = \frac{-1}{R_F C_F} \int_0^t V_i(t)\, dt$$

Thus the circuit provides an output voltage which is proportional to the time integral of the input and $R_1 C_F$ is the time constant of the integrator.

$$V_o(s) = \frac{-1}{sR_1 C_F} [V_i(s)]$$

$s = j\omega$

$$|A| = \frac{V_o(j\omega)}{V_i(j\omega)} = \left| \frac{-1}{j\omega R_1 C_F} \right| = \frac{1}{\omega R_1 C_1}$$

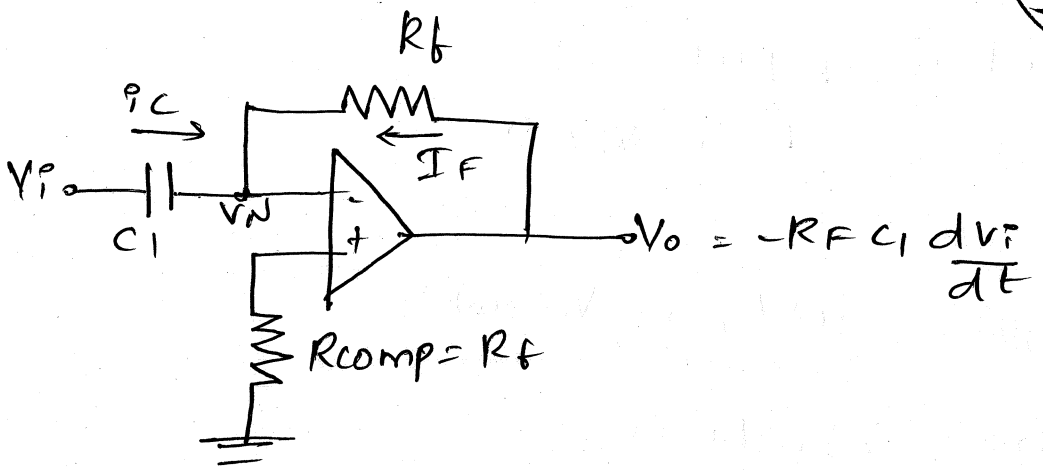
$$= \frac{1}{2\pi f R_1 C_F}$$

$$A = f_b / f$$

$$f = \frac{1}{2\pi R_1 C_F}$$

* At the gain of an integrator decreases with increasing frequency the integrator at does not have any frequency problem as faced in differentiator.

DIFFERENTIATOR:



ANALYSIS:

At node 'N' is virtual ground potential (i.e) $V_N = 0$. The current flow through the capacitor is

$$I_C = C_1 \frac{d}{dt}(V_i - V_N)$$

$$= C_1 \frac{dV_i}{dt} - C_1 \frac{dV_N}{dt}$$

$\therefore V_N = 0$

$$I_C = C_1 \frac{dV_i}{dt}$$

$$I_F = \frac{V_o}{R_F}$$

$$C_1 \frac{dV_i}{dt} + \frac{V_o}{R_F} = 0$$

$$\frac{V_o}{R_F} = -C_1 \frac{dV_i}{dt}$$

$$\boxed{V_o = -R_F C_1 \frac{dV_i}{dt}}$$

The output V_o is a constant $(-R_F C_1)$ times the derivation of input voltage. negative sign indicates 180° phase shift of output V_o with respect to input.

$$V_o(s) = -s R_F C_1 V_i(s)$$

$$s = j\omega$$

$$V_o(j\omega) = -j\omega R_F C_1 V_i(j\omega)$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega R_F C_1$$

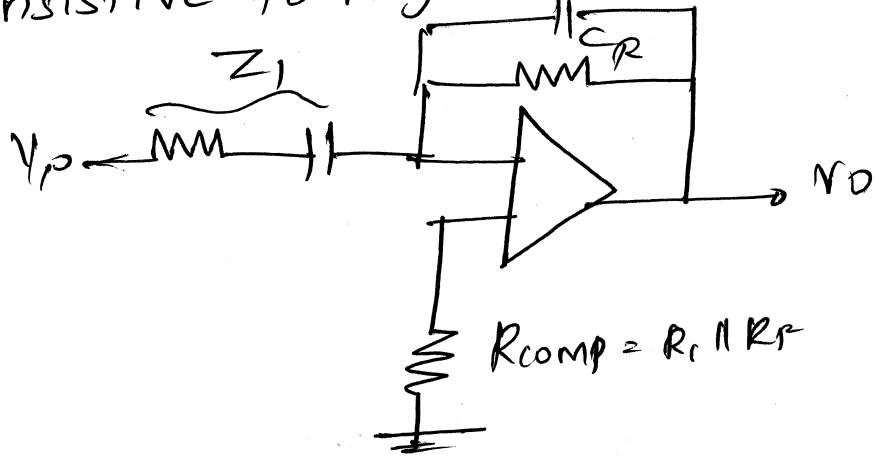
$$|A| = |j\omega R_F C_1|$$

$$A_i = 2\pi f R_F C_1$$

$$|A| = f/f_a \quad \therefore f_a = \frac{1}{2\pi R_F C_1}$$

DRAWBACKS:

1. At high frequency, the ideal differentiator may become unstable and break into oscillation
2. The input impedance decreases with increase in frequency there by making the circuit to sensitive to high frequency noise.



VOLTAGE TO CURRENT CONVERTER (TRANS CONDUCTANCE AMPLIFIER)

* In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuit possible.

→ V-I converter with floating load
→ V-I converter with grounded load.

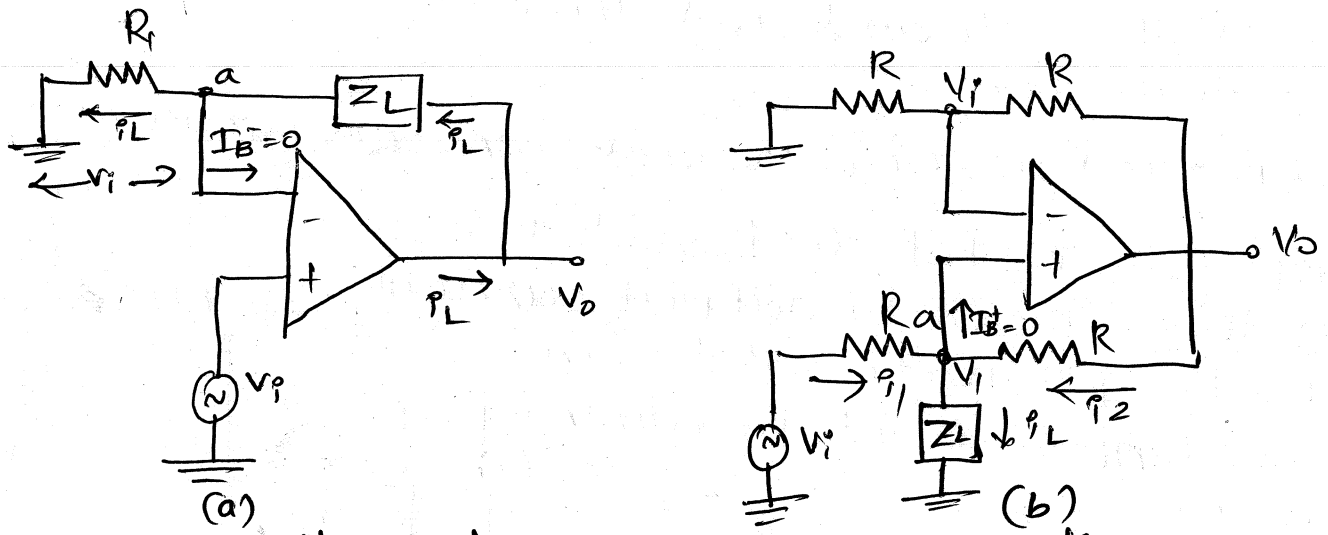


FIG Voltage to current converter with (a) Floating load (b) Grounded load

Figure (a) shows a voltage to current converter in which load Z_L is floating.

$$V_i = i_L R_1$$

$$i_L = \frac{V_i}{R_1}$$

* That is the input voltage V_i is converted into an output current of V_i/R_1.
* It may be seen that the same current flows through the signal source and load
* Signal source should be capable of providing this load current.

$$i_1 + i_2 = i_L$$

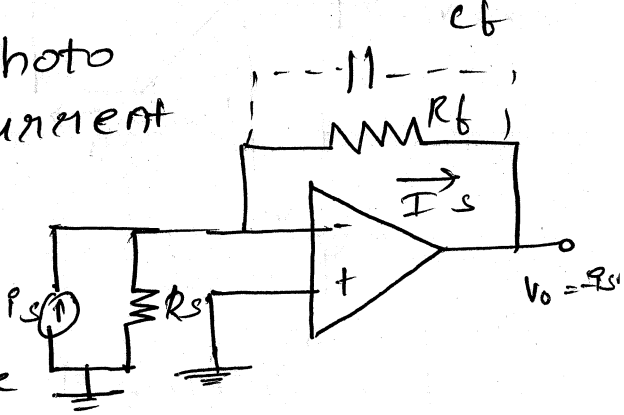
$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o - 2V_1 = i_L R$$

$$V_1 = \frac{V_i + V_o - i_L R}{2}$$

* A Voltage to current converter is used for low Voltage dc and ac Voltmeter, LED and zener diode tester.

CURRENT TO VOLTAGE CONVERTER (TRANSRESISTANCE AMPLIFIER)



* photo cell, photodiode and photo Voltaic cell give an output current that is proportional to an incident radiant energy or light.
* The current through these devices are converted to Voltage by using a current to voltage converter and thereby the amount of light or radiant energy incident on the photodevice can be measured.
* -ve i/p terminal is at virtual ground, no current flows through Rs and current is flows through the feedback resistor.

$$V_o = -i_s R_f$$

Applications:

photo detetors such as photodiodes, photoFETs and photomultipliers.