EE-8451 [LINEAR INTEGRATED CIRCUITS AND APPLICATIONS]
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING.

DACE Cultivating Technology

1. FUNDAMENTALS OF MONOLITHIC IC TECHNOLOGY

REFER: LIC BOOK [Pg.no: 1.5 to 1.20]

* A monolithic circuit, literally speaking means a circuit fabricated from a single stone or a single crystal.
* Monos → Single
  Lithos → Stone
* Advantage: Reducing the cost of production of electronic circuits

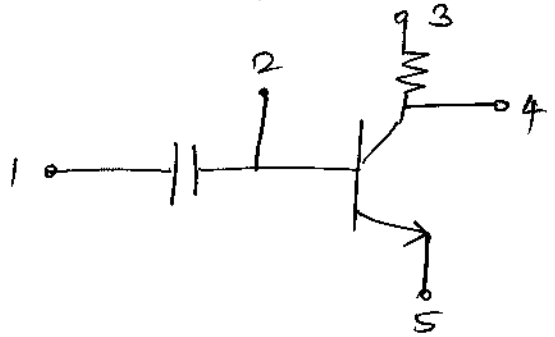


Fig 1. A typical circuit

BASIC PLANAR PROCESSES: (SEOPDIMAA) → FOR REMEMBER

1. Silicon wafer preparation
2. Epitaxial growth
3. Oxidation
4. photolithography
5. Diffusion
6. Ion Implantation
7. Isolation Techniques
8. Metallization
9. Assembly processing and packaging

SILICON WAFER PREPARATION:

Steps used in the preparation of Si-Wafers

1. Crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. Wafer polishing and etching
5. Wafer cleaning.

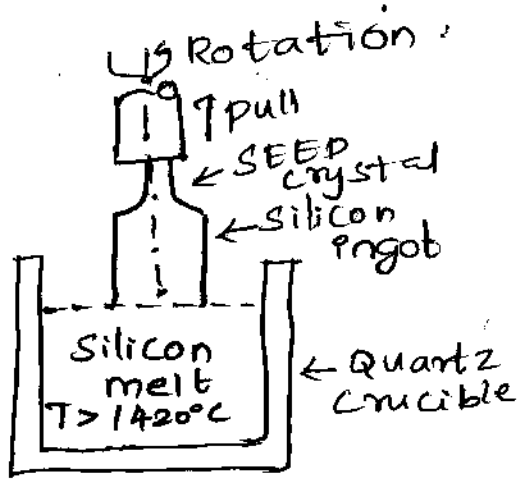


Fig2. Czochralski crystal growth

* Czochralski crystal growth process → used for producing single crystal silicon ingots.

* Poly crystalline silicon + amount of dopant } → put it in a quartz crucible and placed in a furnace

* The material is then heated to a temperature in excess of the silicon melting point of 1420°C
* A small single crystal rod of silicon called a seed crystal is then dipped into the silicon melt and slowly pulled out.
* As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal.
* During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular crossection.
* Top and bottom portions of the ingot are cut off. Ingot surface is ground.

* The silicon wafers so obtained have very rough surface due to slicing operation.
* These wafers undergo a number of polishing steps to produce a flat surface.
* Finally, the wafers are thoroughly rinsed and dried.

EPITAXIAL GROWTH:

* Arranging atoms in single crystal fashion upon a single crystal substrate.

$$SiCl_4 + 2H_2 \underset{}{\overset{1200^\circ C}{\rightleftharpoons}} Si + 4HCl$$

* The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.
* Mostly, epitaxial films with specific impurity concentration are required.

Phosphine → n-type
diborane → p-type
} doping into the silicon tetrachloride hydrogen gas stream.

* Process is carried out in reaction chamber consisting of a long cylindrical quartz tube encircled by an RF induction coil.
* Silicon wafers are placed on a rectangular graphite rod called a boat.
* This boat is then placed in the reaction chamber where the graphite is heated at 1200°C.

OXIDATION:

* SiO_2 has the property of preventing the diffusion of almost all impurities through it.

1. SiO_2 → hard protective coating and is unaffected by almost all reagents except hydrofluoric acid.
2. By selective etching SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

* Silicon wafers are stacked up in a quartz boat and then inserted into a quartz furnace tube.
* The Si-wafers are raised to a high temperature in the range of 950 to 1115°C.

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

* This oxidation process is called thermal oxidation because high temperature is used to grow the oxide layer.

PHOTOLITHOGRAPHY:

* With the help of photolithography, it has become possible to produce microscopically small circuit and device patterns on Si-wafers.

1. Making a photographic mask
2. Photoetching.

The making of a photolithographic mask involves:

* preparation of initial artwork
* Reduction

Preparation of initial artwork:

→ The initial layout or artwork of an IC is normally done at a scale, several hundred times larger than the final dimensions of the finished monolithic circuit.

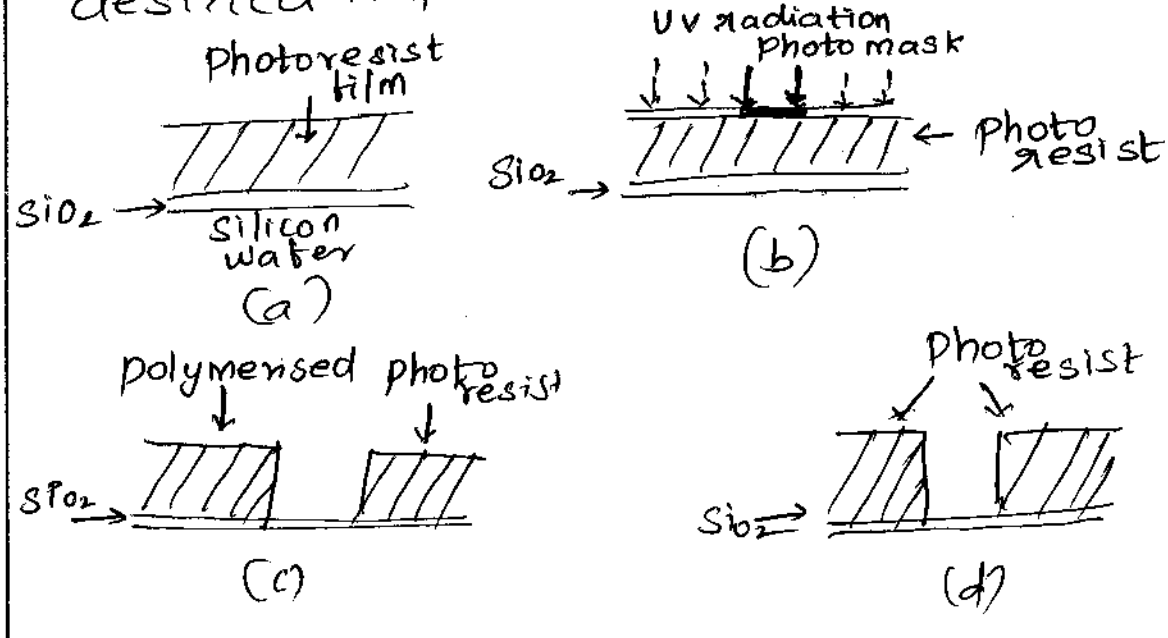
→ This is because, for a tiny chip, larger the artwork, more accurate is the final mask

→ The initial layout is then decomposed into several mask layers, each corresponding to a process step in the Fabrication schedule.

Reduction:

* This rubyth pattern of individual mask is photographed and then reduced in steps by factor 5 to 10 several times to finally obtain the exact image size.

* Photo etching is used for the removal of SiO_2 from desired regions so that desired impurities can be diffused



DIFFUSION:

* This uses a high temperature furnance having a flat temperature profile over a useful length.
* A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1000°C.
* Impurities to be diffused are rarely used in their elemental forms.

B_2O_3, BCl_3 → Sources of Boron

P_2O_5, $POCl_3$ → Sources of Phosphorous

* A carrier gas, such as dry oxygen or nitrogen is normally used for sweeping the impurity to the high temperature zone
* The depth of diffusion depends upon the time of diffusion which normally extends to 2 hours.
* The diffusion of impurities normally takes place both laterally as well as vertically.

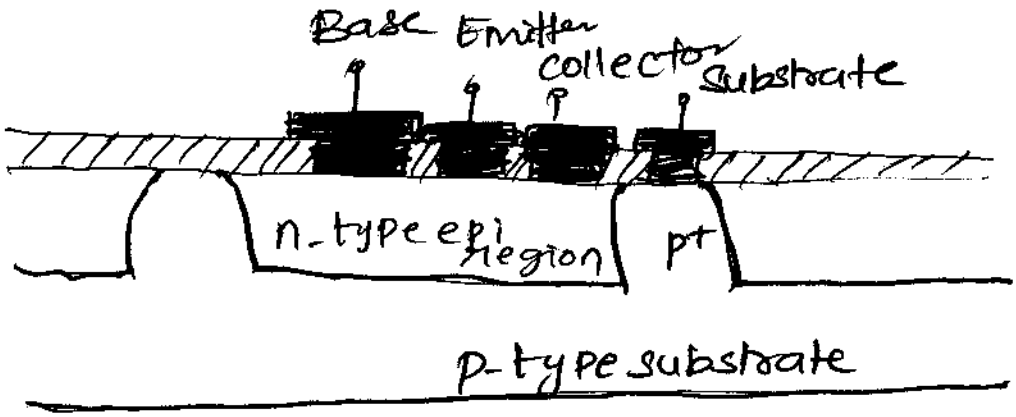


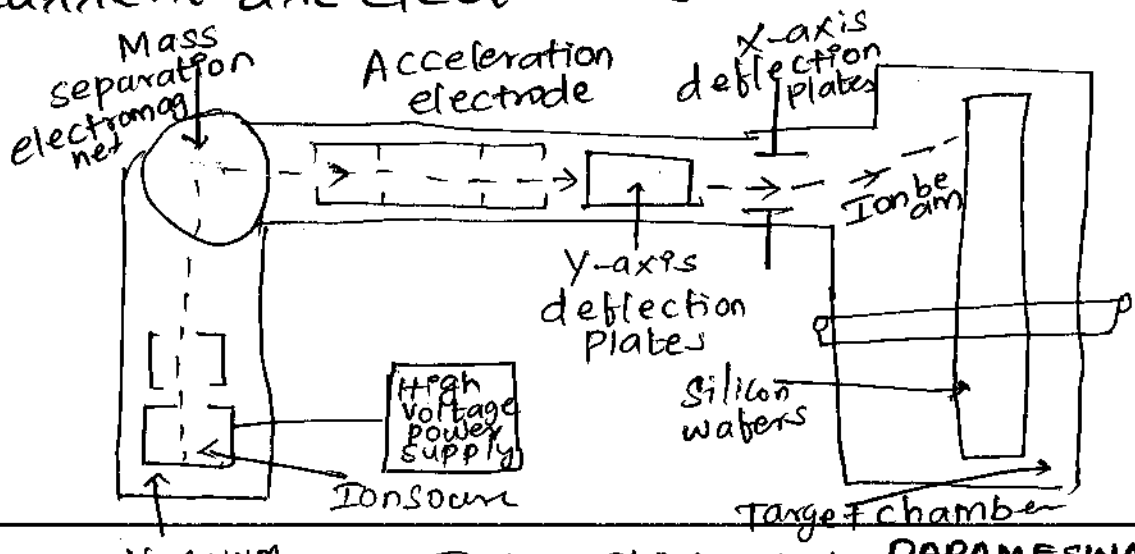
FIG: The cross section of an npn transistor showing curved junction profiles as a result of lateral diffusion.

ION IMPLANTATION:

* It is a technique used to introduce impurities into a silicon wafer.
* Silicon wafers are placed in a vacuum chamber and are scanned by a beam of high energy dopant ions.
* These ions are accelerated by energies between 20 KV to 250 KV.
* As the ion strikes the silicon wafers, they penetrate some small distance into the wafer.
* The depth of penetration of any particular type of ion increases with increasing accelerating voltage.

Advantages:

* It is performed at low temperatures.
* Therefore, previously diffused regions have a lesser tendency for lateral spreading.
* In diffusion process, temperature has to be controlled over a large area inside the oven, where as ion implantation technique, accelerating potential and the beam current are electrically controlled from outside



ION IMPLANTATION PARAMESWARAN.R

ISOLATION TECHNIQUES:

* Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections.

* TYPES OF ISOLATION TECHNIQUES

1. P-n Junction isolation
2. Dielectric isolation

P-n Junction isolation:

* Here, p^+ type impurities are selectively diffused into the n-type epitaxial layer so as to reach p-type substrate.

* If the p-type substrate material is held at the most negative potential in the circuit, the diodes will be reverse biased providing electric isolation between these islands.

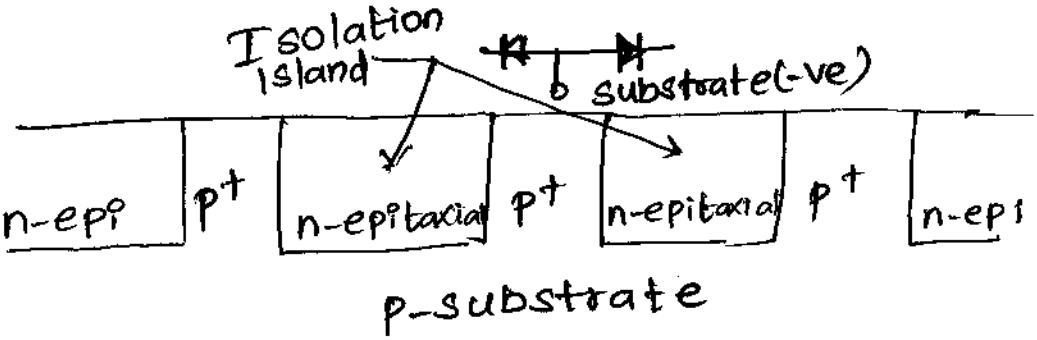


FIG. PN JUNCTION ISOLATION

* The concentration of the acceptor atoms in the region between isolation islands is usually kept much higher than the p-type substrate.

* This prevents the depletion region of the reverse biased diode from penetrating more into p^+ region and possibly connecting the isolation islands.

* It is the presence of a transition capacitance at the isolating pn junctions, resulting in an inevitable capacitor coupling between the components and the substrate.

* These parasitic capacitances limit the performance of a transition circuit at high frequencies

DIELECTRIC ISOLATION:

* A layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation, both electrical and physical.

* This isolating dielectric layer is thick enough so that its associated capacitance is negligible.

* It requires additional fabrication steps, it becomes more expensive.

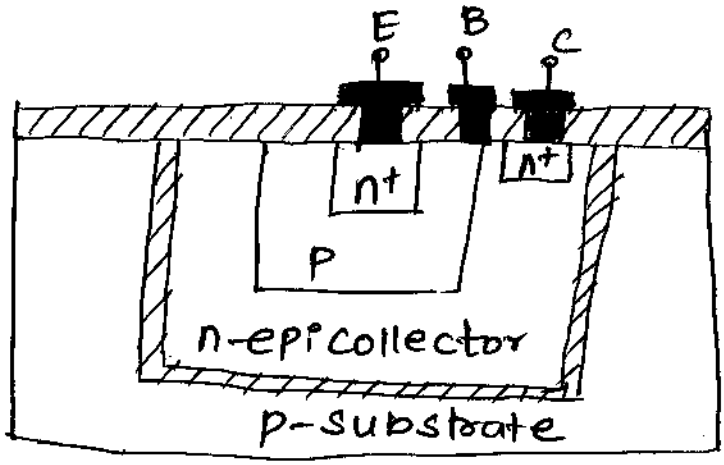


FIG: DIELECTRIC ISOLATION

* The technique is mostly used for fabricating professional grade ICs required for specialised applications.

METALLIZATION:

* The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip.
* Aluminium is usually used for the metallization of most ICs.

1. It is relatively a good conductor
2. It is easy to deposit aluminium films using deposition.
3. Aluminium makes good mechanical bonds with silicon.
4. Aluminium forms low resistance, ohmic contact with p-type silicon and heavily doped n-type silicon.

* The material to be evapora-ted is placed in a resistance heated tungsten coil.
* A very high power density electron beam is focussed at the surface of the material to be evaporated.
* This heats up the material to very high temperature and it starts vaporising. These vapours travel in straight line paths
* The evaporated molecules hit the substrate and condense there to form a thin film coating.

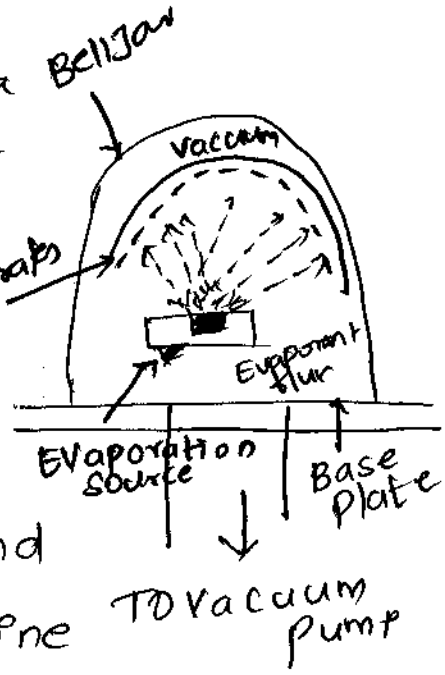


Fig: Vacuum evaporation for metallization

* After the thin film metallization is done, the film is patterned to produce the required interconnections and bonding pad configuration.

ASSEMBLY PROCESSING AND PACKAGING:

* Each of the wafer processed contains several hundred chips, each being a complete circuit.

* A common method called scribing and clea-ving used for separation makes use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips.

There are three different package configurations available:

1. Metal can package
2. ceramic flat package
3. Dual-in-package

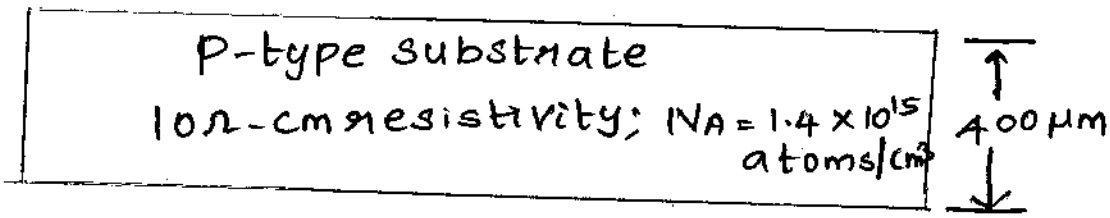
UNIVERSITY QUESTIONS

1. With neat illustrations explain the various steps involved in the IC fabrication process.
2. Describe the steps involved in the fabrication of monolithic transistor
3. Explain the basic process used in silicon planar technology with neat diagram.
4. Write a note on masking and etching process in IC fabrication

2. FABRICATION OF A TYPICAL CIRCUIT:

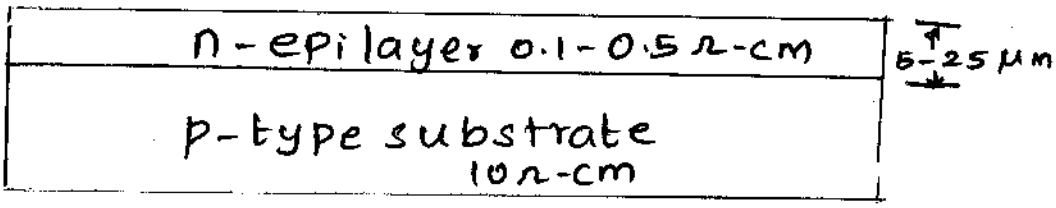
REFER: LIC BOOK [Pg.no: 1.21 to 1.24]

Step1: WAFER PREPARATION



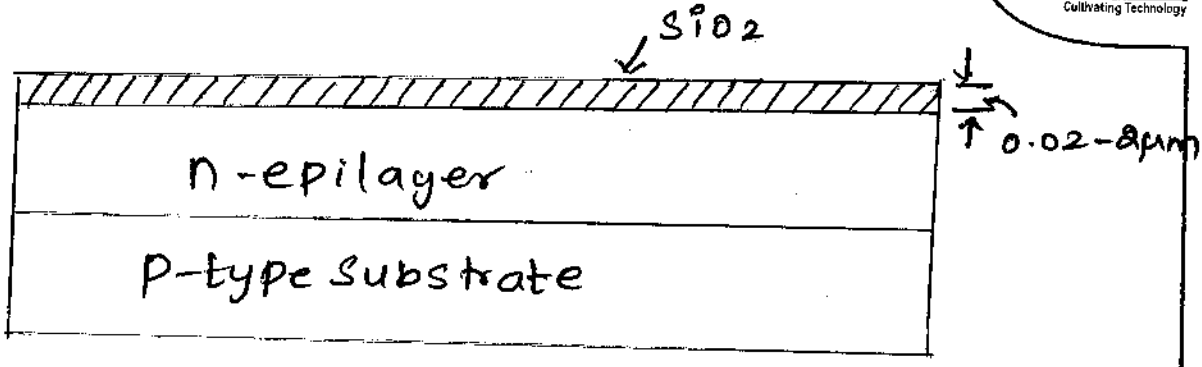
* The starting material called the substrate is a p-type silicon wafer.
* The wafers are usually of 10-cm diameter and 0.4 mm thickness.
* Resistivity = 10Ω-cm
* concentration of acceptor atom = $N_A = 1.4 \times 10^{15}$ atoms/cm3

Step2: EPITAXIAL GROWTH



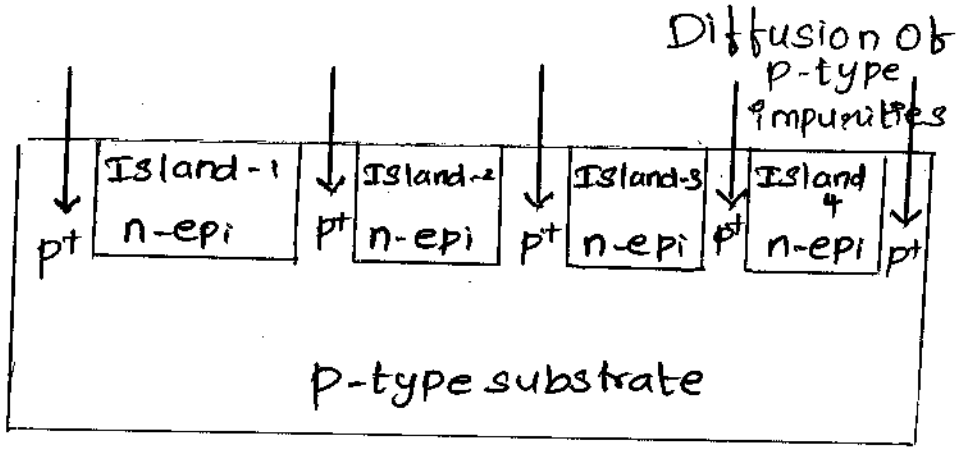
* An n-type epitaxial film is grown on the p-type substrate.
* This ultimately becomes the collector region of the transistor, or an element of the diode and diffused capacitor associated with the circuit.
* Resitivity = 0.1 to 0.5Ω-cm.
* All active and passive layer of components are fabricated within this layer.

Step3: OXIDATION



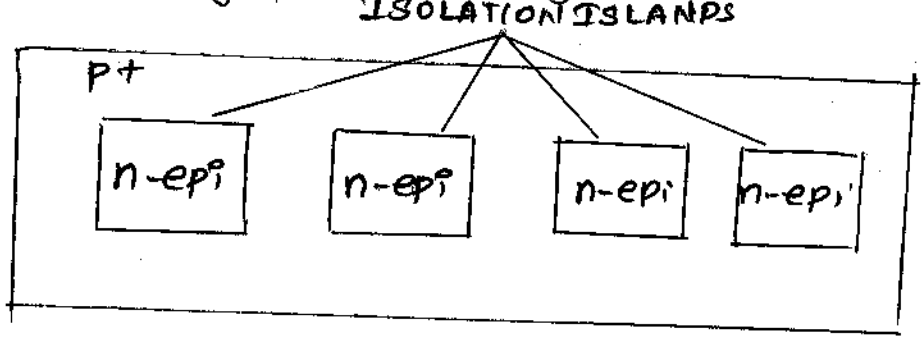
* A SiO_2 layer of thickness of the order of 0.02 to 2 μm.

Step 4: ISOLATION DIFFUSION



* Four components have to be fabricated, so we realize four islands which are isolated.

* SiO_2 is removed from five different Places using photolithographic technique

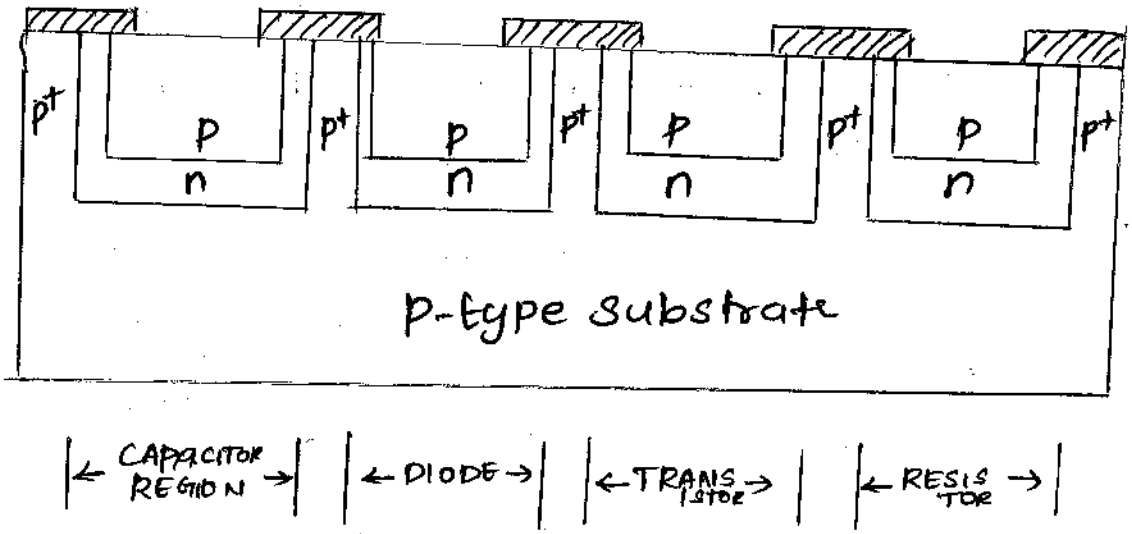


* The area under the SiO_2 are n-type islands that are completely surrounded by p-type moats

* As long as the p-n junction between the isolation

islands are held at reverse bias, that is the p-type substrate is held at negative potential with respect to n-type isolation islands, these regions are electrically isolated from each other by two back to back diodes, providing the desired isolation.

Step:5 : BASE DIFFUSION



* A new layer of SiO_2 is grown over the entire wafer and a new pattern of openings is formed using photolithographic technique.

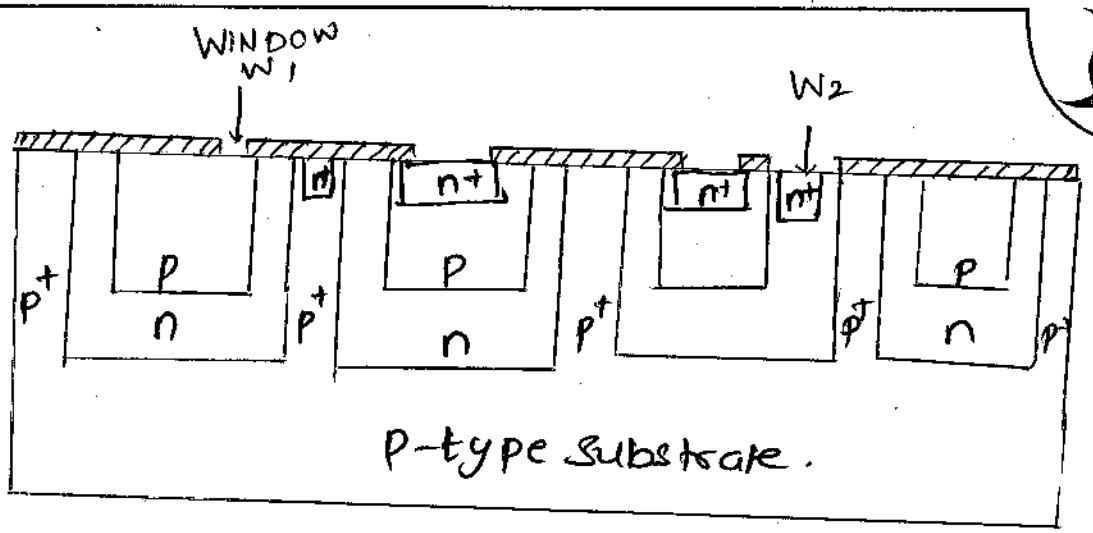
* p-type impurities such as boron are diffused through the openings into the islands of n-type epitaxial silicon.

* The depth of this diffusion must be controlled so that it does not penetrate through n-layer into the substrate.

* This diffusion is utilized to form the base region, transistor, resistor, the anode of the diode and junction capacitor

Step6 : EMITTER DIFFUSION

* A new layer of SiO_2 is again grown over the entire wafer and selectively etched to open a new set of windows and n-type impurity is



* Windows are also etched into n- region where contact is to be made to the n-type layer.

* Aluminium, normally used for making inter connections, is a p-type impurity in silicon and produce an unwanted rectifying contact with the lightly doped n-material.

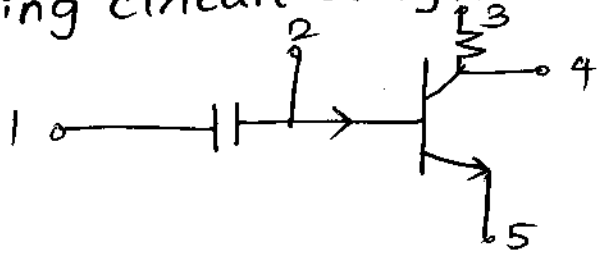
* Thus n^+ layer makes a good ohmic contact with the Al-layer

Step 7: ALUMINIUM METALLIZATION

* IC chip is complete with all active and passive devices between the various compone-nts have to be made in accordance with the circuit.

UNIVERSITY QUESTIONS

1. Describe about epitaxial growth process.
2. Explain in detail about the photolithography process with neat diagram.
3. Explain the fabrication process involved in the following circuit diagram.



3. FABRICATION OF FET:

REFER: LIC BOOK [Pg.no - 1.35 to 1.38]

* FET is a device in which the flow of current through the conducting region is controlled by an electric field.

(i) JFET
(ii) MOSFET

JFET FABRICATION:

* The epitaxial layer which formed the collector of the BJT is used as the n-channel of the JFET.
* The p+ gate is formed in the n-channel by the process of diffusion or ion implantation.
* The n+ regions have been formed under the drain and source contact regions to provide good ohmic contact.

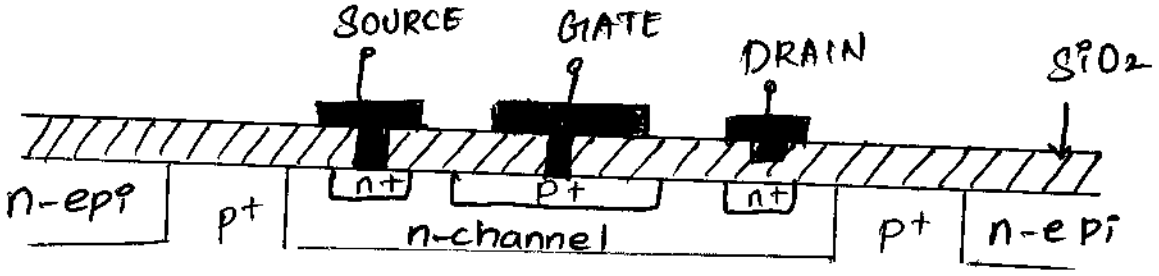


FIG: n-channel JFET structure

MOSFET FABRICATION:

* Enhancement type and depletion type
* Metallic Gate G is separated from the semiconductor channel by the insulating SiO_2 layer.
* The insulating layer of silicon dioxide gives an extremely high input resistance.

Threshold Voltage → 3 to 6V
Power supply → 12 V

USE OF SILICON NITRIDE: (Si_3N_4)

* Si_3N_4 has superior masking properties compared to SiO_2.
* The Si_3N_4 is sandwiched between two SiO_2 layers and provide the necessary barrier to prevent impurities penetrating through the SiO_2 layer.
* dielectric constant of Si_3N_4 → 7.5
* dielectric constant of SiO_2 → 04
* This increased overall dielectric constant reduces V_T.

POLYSILICON GATE:

* Polycrystalline silicon when doped with phosphorus is conductive and is used as the gate electrode instead of aluminium.
* This reduces V_T to about 1 to 2V.
* Such devices are called Silicongate MOS transistors
* Si_3N_4 → Coated to the entire surface of a P-type wafer
* Si_3N_4 → Next to etched away from the surface outside the transistor region.

The two important points to be noticed:

1. The polysilicon-gate provides self-alignment of the gate with the source and drain. The Silicongate due to self-aligning property eliminates these capacitances.
2. No isolation island is required.

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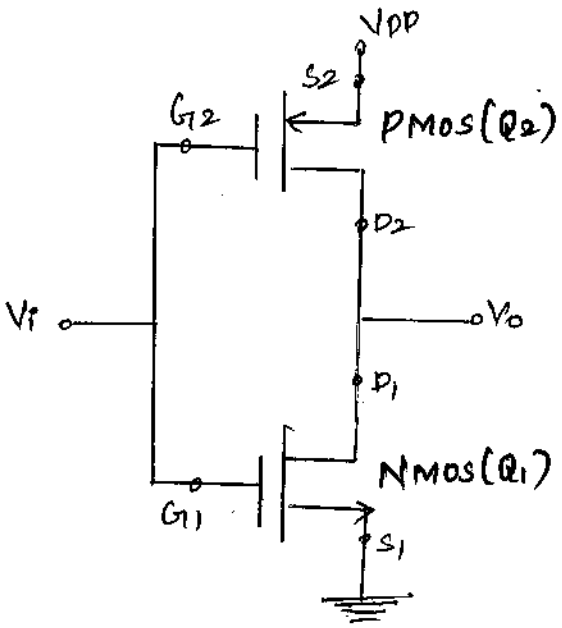
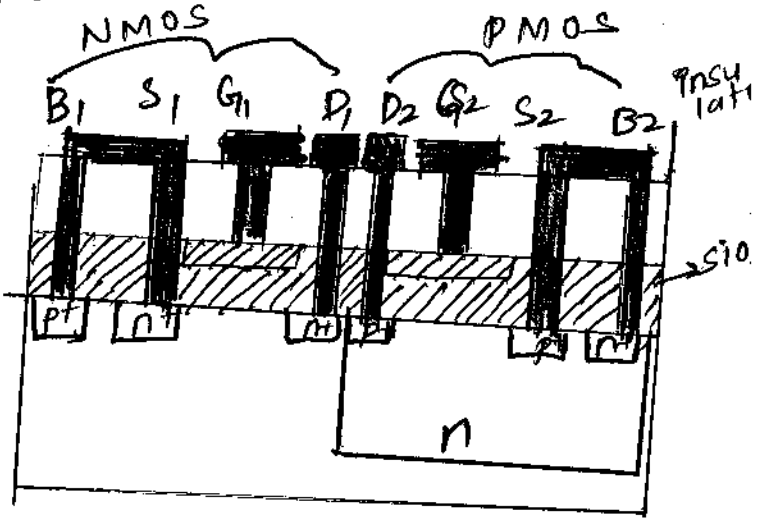
CMOS FABRICATION:

* It is possible to fabricate NMOS and PMOS enhancement devices on the same silicon chip.



FIG(a) CMOS INVERTER



* B_1 is tied to S_1 → connected to the GND
* B_2 is tied to S_2 → supply Voltage VDP
* since, B_1 → p-type
  B_2 → n-type

* Both the substrates are reverse biased and thus cutoff. Thus, isolation between NMOS and PMOS transistor is automatically achieved.

4. THIN AND THICK FILM TECHNOLOGY:

REFER: LIC ROYCHOUDHURY BOOK [Pg.no- 30 to 33]

* Flim technology at present can produce only passive components.

* It will be mainly used for isolation or interconnections have to made in integrated circuits.

FILM ICs

- THINFLIM: Thickness - 50 Å to 20,000 Å
- THICKFILM: Thickness - 1,25,000 Å to 6,25,000 Å

* Thick film ICs are made by the process of screen printing, usually like silk screening techniques

* Thin film materials are generally deposited on to substrates in a vacuum chamber.

* Thick film produces cheap and rugged resi-stors, capacitors and conducting patterns.

* Thin film technology provides greater precision in manufacturing but is more costly than thick film technology.

DEPOSITION OF THINFILM:

1. Vacuum evaporation
2. Sputtering
3. Gas plating
4. Electroplating
5. Electroless plating
6. Silk screening

VACUUM EVAPORATION:

* Thin film metal layer will serve to make interconnections of the various components on the chip.

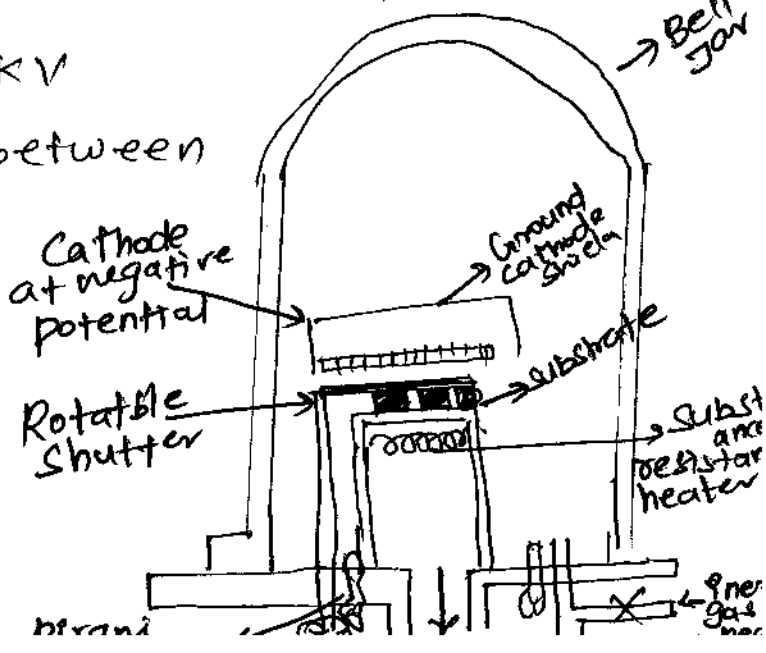
* It is easy to deposit aluminium films using vacuum deposition.

* thickness → 1μm
* conduction width → 2 to 25 μm
* pressure → 10^{-6} to 10^{-9} torr
* The material to be evaporated is placed in a resistance heated tungsten coil.

MORE POINTS WILL BE GIVEN IN METALLIZATION.

CATHODE SPUTTERING:

* It is almost identical to that used for vacuum evaporation.
* much slower process
* performed at low pressure (about 10^{-12} torr)
* Source material → intense bombardment by the ions of a inert gas.
* These gas ions are accelerated.
* potential → 2 to 5 KV
* potential applied between the cathode and anode, and produces a glow discharge that fills the entire interelectrode space



PLATING TECHNIQUE:

(i) Electroplating
(ii) Electroless plating

Electroplating:

* process of coating an object with one or more layers of different metals.
* Substrate and metal → immersed in an electrolytic solution
* dc is passed through it → ions migrated
* This method is suitable for making conduction films of gold or copper.

Electroless plating:

* a metal ion in solution is reduced to the free metal and deposited as a metallic coating without the use of an electric current
* This process can be used to deposit metals on any substrate such as glass, ceramic

THICK FILM TECHNOLOGY:

(i) Screen printing
(ii) Ceramic printing

* The process of screen printing pattern is ancient one
* The screens used are woven from stainless steel wires to mesh size 320 and mounted on aluminium frame so as to keep the under uniform tension.
* The screen is next coated with a photo-sensitive emulsion which polymerizes on exposure to light.

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* A mask of the desired pattern is made and kept on it.
* The screen becomes clear wherever thick film is to be deposited and blocked by the photoresist
* The screen is now placed on a substrate and carefully aligned components are deposited on the substrate through screening process.
* The screening process is carried out by a squeegee driven across the patterned screen at a constant rate.
* The desired physical and electrical properties from the thick films so deposited are now developed by thermal processing usually referred to as firing.
* It uses a furnace or kiln where temperature varies from 500°C to 1000°C
* During the firing process, the organic binders of the thick film paste vaporises and the remaining material fuses with the substrate.

SURFACE MOUNT TECHNOLOGY:

* Advanced achievements in the area of semiconductor technology.
* Improves the product → size and quality
* Automation of manufacturing process as well as interconnection methodology can be achieved.
* SMT utilizes micro-miniature leaded or leadless components called SMD.
* The compact size of SMD components greatly reduce the area in PCB, thus increasing packaging density
* Both the components as well as conductive path are installed on the same side of the PCB.
* In conventional mounting technology, components and conductive paths are different sides of PCB.

5. FABRICATION OF RESISTANCE:

REFER: LIC BOOK [pg.no - 1.31 to 1.34]

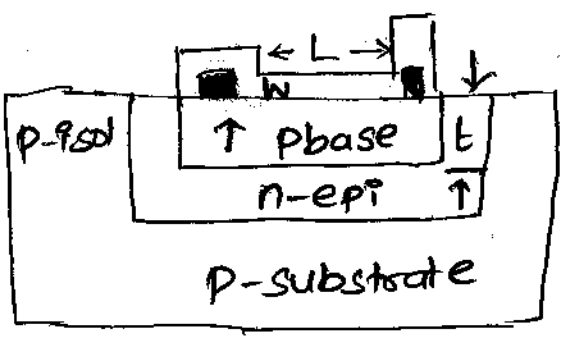
* A resistor in a monolithic integrated circuit is very often obtained by utilizing the bulk resistivity of one of the areas

1. Diffused resistor
2. Epitaxial Resistor
3. pinched Resistor
4. Thin film Resistor

DIFFUSED RESISTOR:

* Diffused resistor is formed in one of the isolated regions of epitaxial layer during base or emitter diffusion.
* As no extra fabricating steps are required, this type of resistors are very economical.
* The value of resistance depends upon the surface geometry (i.e) length and width and upon the diffused impurity profile.
* A very useful quantity sheet is resistance is defined as diffused layers are very thin

$$R = \frac{\rho L}{A} = \frac{\rho L}{L \times t} = \frac{\rho}{t} \text{ (ohms per square)}$$



(a) BASE RESISTOR

* Base resistor in the range of 20Ω to 300KΩ can be easily fabricated due to medium resistivity p-type base region.
* However, the sheet resistance of the emitter diffusion is the order of 5Ω/sq only.

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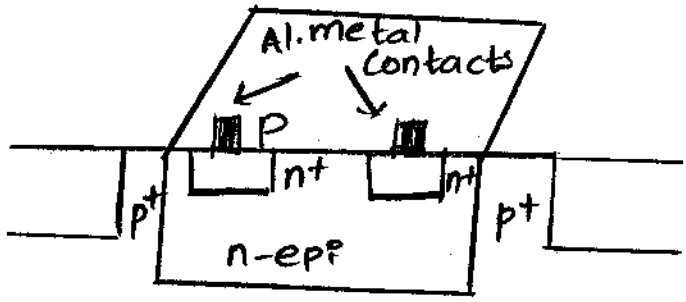
EPITAXIAL RESISTOR:

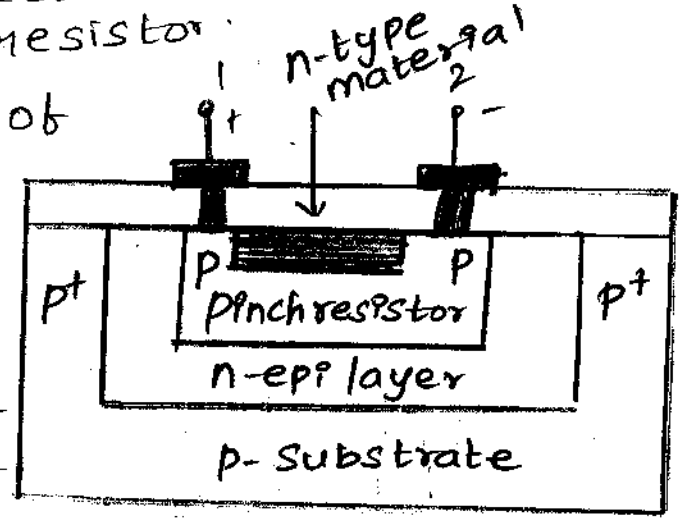
* The N-epitaxial layer can be used for realizing large resistance value by using n-epitaxial collector region.
* Sheet resistance of epitaxial layer in the order of 1 to 10 KΩ/square can be obtained.



STRUCTURE OF EPITAXIAL RESISTOR

PINCHED RESISTOR :

* The sheet of resistivity of a semiconductor can be increased by reducing its effective cross sectional area.
* In a pinched resistor, this technique is used to achieve a high value of sheet resistance from the ordinary base diffused resistor.
* It can offer resistance of the order of mega ohms in a smaller area.
* In the structure shown no current can flow in the N-type material since the diode realized at contact 2 is biased in the reverse direction.

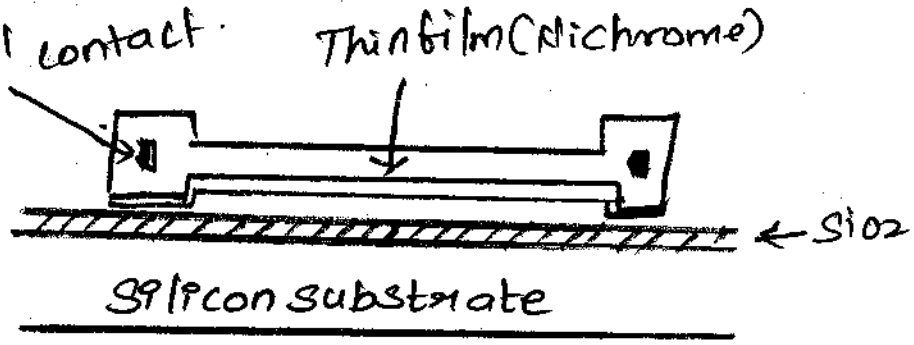


CROSS SECTIONAL VIEW OF PINCH RESISTOR

* only small reverse saturation current can flow in the N-region. Therefore, by forming this N-region in the base diffusion, conduction path for the current has been reduced and pinched.
* The resistance between the contact 1 and 2 increases

THIN FILM RESISTOR:

* Thin metallic film → Nichrome ($NiCr$) of thickness less than 1μm is vapour deposited on the SiO_2 layer.
* Using masked etching, desired geometry of this thin film is achieved to obtain suitable values of resistors.
* The ohmic contacts are made using Al metallization and usual masked etching techniques Nichrome resistors are available with typical sheet resistance values of 40 to 400 Ω/square depending upon film thickness.
* So that resistance in the range of 20 to 50kΩ can be obtained.



ADVANTAGES:

1. They have lesser and small parasitic components and hence their high frealuency behaviour is better.
2. The values of thin film resistors can be easily adjusted even after fabrication by cutting a part of the resistor with a laser beam.
3. They have low temperature coefficient, thereby making them stable.

DISADVANTAGES:

1. Additional steps realuired in their fabrication process.